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Hard Disk Drive Specification

**Deskstar 7K400**

Serial ATA Addendum Interface

Models: HDS724040KLSA80



Version 1.0

05 April 2004

Publication number 2900



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# 1.0 General

## 1.1 Introduction

This specification describes the host interface unique to HDS724040KLSA00 Serial ATA model. The host interface common to both Parallel ATA and Serial ATA is described in the main specification "Hitachi Deskstar 7K00 Specification."

The interface conforms to the Working Document of Information technology - Serial ATA High Speed Serialized AT Attachment Revision 1.0a dated on 7 January 2003 with certain limitations described in 1.3, "Deviations from standard."

## 1.2 Terminology

|               |   |
|---------------|---|
| <b>Device</b> | Device indicates HDS724040KLSA80                          |
| <b>Host</b>   | Host indicates the system that the device is attached to. |

## 1.3 Deviations from standard

The device conforms to the referenced specifications with the following deviations:

|                             |  |
|-----------------------------|--|
| <b>COMReset</b>             | COMReset response is not the same as that of power on reset. Refer to section 3.1, " <u>Reset Response</u> " for detail. |
| <b>Device/Head Register</b> | Device/Head Register bit 5 and 7 are 1   |



## 2.0 Registers

In Serial ATA, the host adapter contains a set of registers that shadow the contents of the traditional device registers, referred to as the Shadow Register Block. Shadow Register Block registers are interface registers used for delivering commands to the device or posting status from the device. About details, please refer to the Serial ATA Spec.

In the following cases, the host adapter sets the BSY bit in its shadow Status Register and then transmits a from to the device containing the new register contents.

- Command register is written in the Shadow Register Block
- Device Control register is written in the Shadow Register Block with a change of state of the SRST bit
- COMRESET is requested

### 2.1 Device/Head Register

**Table 1: Device Head/Register**

|   |   |   |     |     |     |     |     |
|---|---|---|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4   | 3   | 2   | 1   | 0   |
| 1 | L | 1 | DRV | HS3 | HS2 | HS1 | HS0 |

This register contains the device and head numbers. The usage of bit 4 is unique to Serial ATA.

#### **Bit**                      **Definitions**

- L**                      Binary encoded address mode select. When L = 0, addressing is by CHS mode. When L = 1, addressing is by LBA mode.
- DRV**                      This bit is reserved since all Serial ATA devices behave like Device 0 devices.
- HS3, HS2, HS1, HS0**                      Head Select. These four bits indicate the binary encoded address of the head. Bit HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head. The head number may be from zero to the number of heads minus one. In LBA mode, HS3 through HS0 contain bits 24–27 of the LBA. At command completion these bits are updated to reflect the current LBA bits 24–27.



# 3.0 General operation

## 3.1 Reset response

ATA has the following three types of resets:

- Power On Reset (POR)**      The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametric, and sets default values.
- COMRESET**                      COMRESET- signal is negated in Serial ATA Bus. The device resets the interface circuitry as well as Soft Reset.
- Soft Reset (Software Reset)**      SRST bit in the Device Control Register is set, then is reset. The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in the table below.

|   | POR  | COM-RESE | Soft Reset |
|---|------|----------|------------|
| Aborting Host interface                                 | -    | o        | o          |
| Aborting Device operation                               | -    | (*1)     | (*1)       |
| Initialization of hardware                              | o    | x        | x          |
| Internal diagnostic                                     | o    | x        | x          |
| Spinning spindle  | o    | x        | x          |
| Initialization of registers (*2)                        | o    | o        | o          |
| Reverting programmed parameters to default              | o    | (*3)     | (*3)       |
| - Number of CHS<br>(set by Initialize Device Parameter) |      |          |            |
| - Multiple mode   |      |          |            |
| - Write cache   |      |          |            |
| - Read look-ahead                                       |      |          |            |
| - ECC bytes   |      |          |            |
| Disable Standby timer                                   | o    | x        | x          |
| Power mode  | (*5) | (*4)     | (*4)       |

O – execute

X – does not execute

Notes:

- (\*1)      Execute after the data in write cache has been written.
- (\*2)      The default value on POR is shown in Table 2: “Default Register Values” on page 7.
- (\*3)      The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.
- (\*4)      In the case of Sleep mode, the device goes to Standby mode. In other cases, the device does not change current mode.
- (\*5)      Idle when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

## 3.2 Register initialization

After a power on, a hard reset, or a software reset, the register values are initialized as shown in the table below.

**Table 2: Default Register Values**

| Register         | Default Value   |
|------------------|-----------------|
| Error            | Diagnostic Code |
| Sector Count     | 01h             |
| Sector Number    | 01h             |
| Cylinder Low     | 00h             |
| Cylinder High    | 00h             |
| Device/Head      | A0h             |
| Status           | 50h             |
| Alternate Status | 50h             |

After power on, COMRESET, software reset, the register values are initialized as shown in the Default Register Values table.

**Table 3: Diagnostic codes**

| Code | Description                     |
|------|---------------------------------|
| 01h  | No error detected               |
| 02h  | Formatter device error          |
| 03h  | Sector buffer error             |
| 04h  | ECC circuitry error             |
| 05h  | Controller microprocessor error |
| 8xh  | Device 1 failed                 |

The meaning of the Error Register diagnostic codes resulting from the power on, hard reset or the Execute Device Diagnostic command is shown in the Diagnostic codes table.

### **3.3 Diagnostic and Reset considerations**

In each case of Power on Reset, COMRESET, soft reset and the EXECUTE Device DIAGNOSTIC command, the device is diagnosed. And the Error register is set as shown in tables XX, XX

### **3.4 Power Management Mode (Slumber and Partial)**

Power Management Mode is not supported. Device ignores the signals of PMREQ\_S/PMREQ\_P from Host. Please refer to the Serial ATA Specification about Power Management Mode.



## 4.0 Command protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

Please refer to Serial ATA Revision 1.0a (Sector 9. device command layer protocol) about each protocols.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a COMRESET or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

### 4.1 PIO Data In Commands

The following are Data In commands:

- Device Configuration Identity
- Identify Device
- Read Buffer
- Read Log Ext
- Read Long
- Read Multiple
- Read Multiple Ext
- Read Sector(s)
- Read Sector(s) Ext
- Read Stream PIO
- S.M.A.R.T. Read Attribute Values
- S.M.A.R.T. Read Attribute Thresholds
- S.M.A.R.T. Read log sector

Execution includes the transfer of one or more 512 byte (> 512 bytes on Read Long) sectors of data from the device to the host.

### 4.2 PIO Data Out Commands

The following are Data Out commands:

- Device Configuration SET
- Download Microcode
- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password

- Security Unlock
- Set Max Set Password
- Set Max Unlock
- S.M.A.R.T. Write log sector
- Write Buffer
- Write Log Ext
- Write Long
- Write Multiple
- Write Multiple Ext
- Write Sector(s)
- Write Sector(s) Ext
- Write Stream PIO

Execution includes the transfer of one or more 512 byte (> 512 bytes on Write Long) sectors of data from the host to the device.

### **4.3 Non-data commands**

The following are Non-data commands:

- Check Power Mode
- Device Configuration FREEZE LOCK
- Device Configuration RESTORE
- Execute Device Diagnostic
- Flush Cache
- Flush Cache Ext
- Idle
- Idle Immediate
- Initialize Device Parameters
- NOP
- Read Native Max ADDRESS
- Read Native Max ADDRESS Ext
- Read Verify Sector(s)
- Read Verify Sector(s) Ext
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max ADDRESS
- Set Max ADDRESS Ext
- Set Max LOCK command
- Set Max FREEZE LOCK command
- Set Multiple Mode
- Sleep
- S.M.A.R.T. Disable Operations

- S.M.A.R.T. Enable/Disable Attribute Autosave
- S.M.A.R.T. Enable/Disable Automatic Off Line
- S.M.A.R.T. Enable Operations
- S.M.A.R.T. Execute Off-line Data Collection
- S.M.A.R.T. Return Status
- S.M.A.R.T. Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer:

## 4.4 DMA data in Commands

These commands are:

- Read DMA
- Read DMA Ext

## 4.5 DMA data out Commands

These commands are:

- Write DMA
- Write DMA Ext

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device using DMA transfer. A single interrupt is issued at the completion of the successful transfer of all data required by the command.

## 4.6 DMA queued commands

DMA queued commands are

- Read DMA Queued
- Read DMA Queued Ext

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host using DMA transfer. All data for the command may be transferred without a bus release between the command receipt and the data transfer. This command may bus release before transferring data. The host shall initialize the DMA controller prior to transferring data. When data transfer is begun, all data for the request shall be transferred without a bus release.

### 4.6.1 Write DMA Queued Commands

These commands are:

- Write DMA Queued
- Write DMA Queued Ext

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host using DMA transfer. All data for the command may be transferred without a bus release between the command receipt and the data transfer. This command may bus release before transferring data. The host shall initialize the DMA controller prior to transferring data. When data transfer is begun, all data for the request shall be transferred without a bus release.

## 4.6.2 Service Commands

This command is:

- Service

## 5.0 Command descriptions

This section only describes the differences of the commands from Parallel ATA interface. The main differences are the following.

- Do not support Streaming feature set
- Only support 4 bytes ECC length for Read / Write Long Commands
- Do not support Ultra DMA mode 6

The following symbols are used in the command descriptions.

### Output registers

- 0** This indicates that the bit must be set to 0.
- 1** This indicates that the bit must be set to 1.
- D** The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.
- H** Head number. This indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
- L** LBA mode. This indicates the addressing mode. Zero specifies CHS mode and one specifies LBA addressing mode.
- R** Retry. Original meaning is already obsolete, there is no difference between 0 and 1. (Using 0 is recommended for future compatibility.)
- B** Option Bit. This indicates that the Option Bit of the Sector Count Register be specified. (This bit is used by Set Max ADDRESS command.)
- V** Valid. This indicates that the bit is part of an output parameter and should be specified.
- x** This indicates that the hex character is not used.
- This indicates that the bit is not used.

### Input registers

- 0** This indicates that the bit is always set to 0.
- 1** This indicates that the bit is always set to 1.
- H** Head number. This indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
- V** Valid. This indicates that the bit is part of an input parameter and will be set by the device to 0 or 1.
- N** Not recommended condition for start up. Indicates that the condition of the device is not recommended for start up.
- This indicates that the bit is not part of an input parameter. Symbols are used in the command descriptions:

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

Serial ATA Device/Head register 4 bit (D) is different from Parallel ATA. In Serial ATA, Device/Head register 4 bit is reserved for all commands. Please refer to the 7K400 Specification about other commands' descriptions which are not described in this Addendum.

## 5.1 Identify Device (ECh)

Table 4: Identify Device command (ECh)

| Command Block Output Registers |   |   |   |   |   |   |   | Command Block Input Registers |               |           |   |   |   |   |   |   |   |
|--------------------------------|---|---|---|---|---|---|---|-------------------------------|---------------|-----------|---|---|---|---|---|---|---|
| Register                       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                             | Register      | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Data                           | - | - | - | - | - | - | - | -                             | Data          | -         | - | - | - | - | - | - | - |
| Feature                        | - | - | - | - | - | - | - | -                             | Error         | see below |   |   |   |   |   |   |   |
| Sector Count                   | - | - | - | - | - | - | - | -                             | Sector Count  | -         | - | - | - | - | - | - | - |
| Sector Number                  | - | - | - | - | - | - | - | -                             | Sector Number | -         | - | - | - | - | - | - | - |
| Cylinder Low                   | - | - | - | - | - | - | - | -                             | Cylinder Low  | -         | - | - | - | - | - | - | - |
| Cylinder High                  | - | - | - | - | - | - | - | -                             | Cylinder High | -         | - | - | - | - | - | - | - |
| Device/Head                    | 1 | - | 1 | D | - | - | - | -                             | Device/Head   | -         | - | - | - | - | - | - | - |
| Command                        | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0                             | Status        | see below |   |   |   |   |   |   |   |

| Error Register |     |   |     |   |     |     |     | Status Register |     |    |     |     |     |     |     |
|----------------|-----|---|-----|---|-----|-----|-----|-----------------|-----|----|-----|-----|-----|-----|-----|
| 7              | 6   | 5 | 4   | 3 | 2   | 1   | 0   | 7               | 6   | 5  | 4   | 3   | 2   | 1   | 0   |
| CRC            | UNC | 0 | IDN | 0 | ABT | TON | AMN | BSY             | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0              | 0   | 0 | 0   | 0 | V   | 0   | 0   | 0               | V   | 0  | -   | -   | 0   | -   | V   |

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Table 5 beginning on page 16.

**Table 5: Identify device information (Part 1 of 7)**

| Word | Content | Description  |
|------|---------|--|
| 22   | 0004H   | Number of ECC bytes (= 4)  |
| 76   | 0002H   | Serial ATA capabilities  |
|      |         | 15-2(=0) Reserved  |
|      |         | 1 (=1) SATA Generation 1   |
|      |         | 0 (=1) Reserved  |
| 84   | 4123H   | Command set/feature supported extensions                               |
|      |         | 15-14(=01) Word84 is valid   |
|      |         | 13-11(=0) Reserved   |
|      |         | 10 (=0) URG bit supported for WRITE STREAM DMA and WRITE STREAM PIO    |
|      |         | 9 (=0) URG bit supported for READ STREAM DMA and READ STREAM PIO       |
|      |         | 8 (=1) World wide name supported                                       |
|      |         | 7 (=0) WRITE DMA QUEUED FUA EXT command supported                      |
|      |         | 6 (=0) WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported |
|      |         | 5 (=1) General Purpose Logging feature set supported                   |
|      |         | 4 (=0) Streaming feature set supported                                 |
|      |         | 3 (=0) Media Card Pass Through Command feature set supported           |
|      |         | 2 (=0) Media serial number supported                                   |
|      |         | 1 (=1) SMART self-test supported                                       |
|      |         | 0 (=1) SMART error logging supported                                   |
| 87   | 4123H   | Command set/feature default  |
|      |         | 15-14(=01) Word 87 is valid  |
|      |         | 13-11 (=0) Reserved  |
|      |         | 10 (=0) URG bit supported for WRITE STREAM DMA and WRITE STREAM PIO    |
|      |         | 9 (=0) URG bit supported for READ STREAM DMA and READ STREAM PIO       |
|      |         | 8 (=1) World wide name supported                                       |
|      |         | 7 (=0) WRITE DMA QUEUED FUA EXT command supported                      |
|      |         | 6 (=0) WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported |
|      |         | 5 (=1) General Purpose Logging feature set supported                   |
|      |         | 4 (=0) Valid CONFIGURE STREAM command has been executed                |

|       |       |  |   |                           |
|-------|-------|--|---|---------------------------|
|       |       | 3 (=0)                                 | Media Card Pass Through Command feature set enabled |                           |
|       |       | 2 (=0)                                 | Media serial number is valid                        |                           |
| 88    | xx3FH | Ultra DMA Transfer modes               |   |                           |
|       |       | 15- 8(=xx)                             | Current active Ultra DMA transfer mode              |                           |
|       |       | 15                                     | Reserved (=0)                                       |                           |
|       |       | 14                                     | Reserved (=0)                                       |                           |
|       |       | 13                                     | Mode 5  | 1 = Active 0 = Not Active |
|       |       | 12                                     | Mode 4  | 1 = Active 0 = Not Active |
|       |       | 11                                     | Mode 3  | 1 = Active 0 = Not Active |
|       |       | 10                                     | Mode 2  | 1 = Active 0 = Not Active |
|       |       | 9                                      | Mode 1  | 1 = Active 0 = Not Active |
|       |       | 8                                      | Mode 0  | 1 = Active 0 = Not Active |
|       |       | 7- 0(=7F)                              | Ultra DMA transfer mode supported                   |                           |
|       |       | 7                                      | Reserved (=0)                                       |                           |
|       |       | 6                                      | Reserved (=0)                                       |                           |
|       |       | 5                                      | Mode 5  | 1 = Support               |
|       |       | 4                                      | Mode 4  | 1 = Support               |
|       |       | 3                                      | Mode 3  | 1 = Support               |
|       |       | 2                                      | Mode 2  | 1 = Support               |
|       |       | 1                                      | Mode 1  | 1 = Support               |
|       |       | 0                                      | Mode 0  | 1 = Support               |
| 93    | 0000H | COMRESET result (= 0)                  |   |                           |
| 95    | 0000H | Stream Minimum Request Size            |   |                           |
| 96    | 0000H | Streaming Transfer Time - DMA          |   |                           |
| 97    | 0000H | Streaming Access Latency - DMA and PIO |   |                           |
| 98-99 | 0000H | Streaming Performance Granularity      |   |                           |
| 104   | 0000H | Streaming Transfer Time - PIO          |   |                           |

## 5.2 Read Log Ext (2Fh)

Table 6: Read Log Ext Command (2Fh)

| Command Block Output Registers |          |   |   |   |   |   |   |   | Command Block Input Registers |               |                 |   |   |   |   |   |   |   |   |
|--------------------------------|----------|---|---|---|---|---|---|---|-------------------------------|---------------|-----------------|---|---|---|---|---|---|---|---|
| Register                       |          | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                             | Register      |                 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Data Low                       |          | - | - | - | - | - | - | - | -                             | Data Low      |                 | - | - | - | - | - | - | - | - |
| Data High                      |          | - | - | - | - | - | - | - | -                             | Data High     |                 | - | - | - | - | - | - | - | - |
| Feature                        | Current  | - | - | - | - | - | - | - | -                             | Error         | ...See Below... |   |   |   |   |   |   |   |   |
|                                | Previous | - | - | - | - | - | - | - | -                             |               |                 |   |   |   |   |   |   |   |   |
| Sector Count                   | Current  | V | V | V | V | V | V | V | V                             | Sector Count  | HOB=0           | - | - | - | - | - | - | - | - |
|                                | Previous | V | V | V | V | V | V | V | V                             |               | HOB=1           | - | - | - | - | - | - | - | - |
| Sector Number                  | Current  | V | V | V | V | V | V | V | V                             | Sector Number | HOB=0           | - | - | - | - | - | - | - | - |
|                                | Previous | - | - | - | - | - | - | - | -                             |               | HOB=1           | - | - | - | - | - | - | - | - |
| Cylinder Low                   | Current  | V | V | V | V | V | V | V | V                             | Cylinder Low  | HOB=0           | - | - | - | - | - | - | - | - |
|                                | Previous | V | V | V | V | V | V | V | V                             |               | HOB=1           | - | - | - | - | - | - | - | - |
| Cylinder High                  | Current  | - | - | - | - | - | - | - | -                             | Cylinder High | HOB=0           | - | - | - | - | - | - | - | - |
|                                | Previous | - | - | - | - | - | - | - | -                             |               | HOB=1           | - | - | - | - | - | - | - | - |
| Device/Head                    |          | 1 | - | 1 | D | - | - | - | -                             | Device/Head   |                 | - | - | - | - | - | - | - | - |
| Command                        |          | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1                             | Status        | ...See Below... |   |   |   |   |   |   |   |   |

| Error Register |     |   |     |   |     |     |     | Status Register |     |    |     |     |     |     |     |
|----------------|-----|---|-----|---|-----|-----|-----|-----------------|-----|----|-----|-----|-----|-----|-----|
| 7              | 6   | 5 | 4   | 3 | 2   | 1   | 0   | 7               | 6   | 5  | 4   | 3   | 2   | 1   | 0   |
| CRC            | UNC | 0 | IDN | 0 | ABT | TON | AMN | BSY             | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0              | V   | 0 | V   | 0 | V   | 0   | 0   | 0               | V   | 0  | V   | -   | 0   | -   | V   |

This command returns the specified log to the host. The device shall interrupt for each DRQ block transferred.

### Output parameters to the device

- Sector Count Current** The number of sectors to be read from the specified log low order, bits (7:0). The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.
- Sector Number Previous** The number of sectors to be read from the specified log high orders, bits (15:8).
- Sector Number Current** The log to be returned as described in the figure below.
- Cylinder Low Current** The first sector of the log to be read low order, bits (7:0).
- Cylinder Low Previous** The first sector of the log to be read high order, bits (15:8).

When the following Log addresses are specified by the host, the Serial ATA device sets ABT bit in the Error register. When other Log addresses are specified, the Serial ATA device executes the command same as Parallel ATA device.

**Table 7: Log Address Definition**

| Log address | Content                   | Feature set | Type      |
|-------------|---------------------------|-------------|-----------|
| 20h         | Streaming Performance log | Streaming   | Read Only |
| 21h         | Write Stream Error log    | Streaming   | Read Only |
| 22h         | Read Stream Error log     | Streaming   | Read Only |

## 5.3 Read Long (22h/23h)

Table 8: Read Long (22h/23h)

| Command Block Output Registers |   |   |   |   |   |   |   | Command Block Input Registers |               |           |   |   |   |   |   |   |   |
|--------------------------------|---|---|---|---|---|---|---|-------------------------------|---------------|-----------|---|---|---|---|---|---|---|
| Register                       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                             | Register      | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Data                           | - | - | - | - | - | - | - | -                             | Data          | -         | - | - | - | - | - | - | - |
| Feature                        | - | - | - | - | - | - | - | -                             | Error         | see below |   |   |   |   |   |   |   |
| Sector Count                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1                             | Sector Count  | -         | - | - | - | - | - | - | V |
| Sector Number                  | V | V | V | V | V | V | V | V                             | Sector Number | V         | V | V | V | V | V | V | V |
| Cylinder Low                   | V | V | V | V | V | V | V | V                             | Cylinder Low  | V         | V | V | V | V | V | V | V |
| Cylinder High                  | V | V | V | V | V | V | V | V                             | Cylinder High | V         | V | V | V | V | V | V | V |
| Device/Head                    | 1 | L | 1 | D | H | H | H | H                             | Device/Head   | -         | - | - | - | H | H | H | H |
| Command                        | 0 | 0 | 1 | 0 | 0 | 0 | 1 | R                             | Status        | see below |   |   |   |   |   |   |   |

| Error Register |     |   |     |   |     |     |     | Status Register |     |    |     |     |     |     |     |
|----------------|-----|---|-----|---|-----|-----|-----|-----------------|-----|----|-----|-----|-----|-----|-----|
| 7              | 6   | 5 | 4   | 3 | 2   | 1   | 0   | 7               | 6   | 5  | 4   | 3   | 2   | 1   | 0   |
| CRC            | UNC | 0 | IDN | 0 | ABT | T0N | AMN | BSY             | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0              | 0   | 0 | V   | 0 | V   | 0   | 0   | 0               | V   | 0  | V   | -   | 0   | -   | V   |

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media. It then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 40 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

### Output parameters to the device

- Sector Count** This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** This indicates the sector number of the sector to be transferred. (L = 0)  
In LBA mode, this register contains LBA bits 0–7. (L = 1)
- Cylinder High/Low** This indicates the cylinder number of the sector to be transferred. (L = 0)  
In LBA mode, this register contains LBA bits 8–15 (Low), 16–23 (High). (L = 1)
- H** This indicates the head number of the sector to be transferred. (L = 0)  
In LBA mode, this register contains LBA bits 24–27. (L = 1)
- R** This indicates the retry bit. This bit is ignored.

### **Input parameters from the device**

- Sector Count** This indicates the number of requested sectors not transferred
- Sector Number** This indicates the sector number of the transferred sector. (L = 0)  
In LBA mode, this register contains current LBA bits 0–7. (L = 1)
- Cylinder High/Low** This indicates the cylinder number of the transferred sector. (L = 0)  
In LBA mode, this register contains current LBA bits 8–15 (Low), 16–23 (High). (L = 1)
- H** This indicates the head number of the transferred sector. (L = 0)  
In LBA mode, this register contains current LBA bits 24–27. (L = 1)

## 5.4 Set Features (EFh)

Table 9: Set Features command (EFh)

| Command Block Output Registers |   |   |   |   |   |   |   | Command Block Input Registers |               |           |   |   |   |   |   |   |   |
|--------------------------------|---|---|---|---|---|---|---|-------------------------------|---------------|-----------|---|---|---|---|---|---|---|
| Register                       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                             | Register      | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Data                           | - | - | - | - | - | - | - | -                             | Data          | -         | - | - | - | - | - | - | - |
| Feature                        | V | V | V | V | V | V | V | V                             | Error         | see below |   |   |   |   |   |   |   |
| Sector Count                   | V | V | V | V | V | V | V | V                             | Sector Count  | -         | - | - | - | - | - | - | - |
| Sector Number                  | - | - | - | - | - | - | - | -                             | Sector Number | -         | - | - | - | - | - | - | - |
| Cylinder Low                   | - | - | - | - | - | - | - | -                             | Cylinder Low  | -         | - | - | - | - | - | - | - |
| Cylinder High                  | - | - | - | - | - | - | - | -                             | Cylinder High | -         | - | - | - | - | - | - | - |
| Device/Head                    | 1 | - | 1 | D | - | - | - | -                             | Device/Head   | -         | - | - | - | - | - | - | - |
| Command                        | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1                             | Status        | see below |   |   |   |   |   |   |   |

| Error Register |     |   |     |   |     |     |     | Status Register |     |    |     |     |     |     |     |
|----------------|-----|---|-----|---|-----|-----|-----|-----------------|-----|----|-----|-----|-----|-----|-----|
| 7              | 6   | 5 | 4   | 3 | 2   | 1   | 0   | 7               | 6   | 5  | 4   | 3   | 2   | 1   | 0   |
| CRC            | UNC | 0 | IDN | 0 | ABT | T0N | AMN | BSY             | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0              | 0   | 0 | 0   | 0 | V   | 0   | 0   | 0               | V   | 0  | -   | -   | 0   | -   | V   |

The Set Feature command establishes the following parameters which affect the execution of certain features as shown in the table below.

The Serial ATA device set ABT to 1 in the Error Register if the Feature register contains following values, since the Serial ATA device only supports 4 byte ECC length for Read/Write Long commands and does not support Streaming feature set.

### Output parameters to the device

```

Feature          Destination code for this command

43H  Set Maximum Host Interface Sector Time
44H  bytes of ECC apply on Read Long/Write Long commands
BBH  4 bytes of ECC apply on Read Long/Write Long commands

```

### 5.4.1 Set Transfer mode

When the type of transfer is Ultra DMA, the maximum mode is 5 in the Serial ATA device.

```
Ultra DMA mode x          01000 nnn (nnn=000,001,010,011,100,101)
```

## 5.5 Write Long (32h/33h)

Table 10: Write Long (32h/33h)

| Command Block Output Registers |   |   |   |   |   |   |   | Command Block Input Registers |               |           |   |   |   |   |   |   |   |
|--------------------------------|---|---|---|---|---|---|---|-------------------------------|---------------|-----------|---|---|---|---|---|---|---|
| Register                       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                             | Register      | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Data                           | - | - | - | - | - | - | - | -                             | Data          | -         | - | - | - | - | - | - | - |
| Feature                        | - | - | - | - | - | - | - | -                             | Error         | see below |   |   |   |   |   |   |   |
| Sector Count                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1                             | Sector Count  | -         | - | - | - | - | - | - | V |
| Sector Number                  | V | V | V | V | V | V | V | V                             | Sector Number | V         | V | V | V | V | V | V | V |
| Cylinder Low                   | V | V | V | V | V | V | V | V                             | Cylinder Low  | V         | V | V | V | V | V | V | V |
| Cylinder High                  | V | V | V | V | V | V | V | V                             | Cylinder High | V         | V | V | V | V | V | V | V |
| Device/Head                    | 1 | L | 1 | D | H | H | H | H                             | Device/Head   | -         | - | - | - | H | H | H | H |
| Command                        | 0 | 0 | 1 | 1 | 0 | 0 | 1 | R                             | Status        | see below |   |   |   |   |   |   |   |

| Error Register |     |   |     |   |     |     |     | Status Register |     |    |     |     |     |     |     |
|----------------|-----|---|-----|---|-----|-----|-----|-----------------|-----|----|-----|-----|-----|-----|-----|
| 7              | 6   | 5 | 4   | 3 | 2   | 1   | 0   | 7               | 6   | 5  | 4   | 3   | 2   | 1   | 0   |
| CRC            | UNC | 0 | IDN | 0 | ABT | T0N | AMN | BSY             | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0              | 0   | 0 | V   | 0 | V   | 0   | 0   | 0               | V   | 0  | V   | -   | 0   | -   | V   |

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are either 4.

### Output parameters to the device

- Sector Count** This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** This indicates the sector number of the sector to be transferred. (L = 0)  
In LBA mode this register contains the LBA bits 0–7. (L = 1)
- Cylinder High/Low** This indicates the cylinder number of the sector to be transferred. (L = 0)  
In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High) (L = 1)
- H** This indicates the head number of the sector to be transferred. (L = 0)  
In LBA mode this register contains the LBA bits 24–27. (L = 1)
- R** The retry bit. This bit is ignored.

### Input parameters from the device

- Sector Count** This indicates the number of requested sectors not transferred.
- Sector Number** This indicates the sector number of the sector to be transferred. (L = 0)  
In LBA mode this register contains the current LBA bits 0–7. (L = 1)
- Cylinder High/Low** This indicates the cylinder number of the sector to be transferred. (L = 0)  
In LBA mode this register contains current the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
- H** This indicates the head number of the sector to be transferred. (L = 0)  
In LBA mode this register contains current the LBA bits 24–27. (L = 1)

## 5.6 Streaming feature commands

The device abort the following commands for Streaming feature set.

- Configure Stream (51h)
- Read Log Ext for Streaming Logs
- Set Features for Set Maximum Host Interface Sector Time
- Read Stream PIO (2Bh)
- Write Stream PIO (3Bh)
- Read Stream DMA (2Ah)
- Write Stream DMA (3Ah)

Both Read Log Ext and Set Features for Streaming feature set is described in the command description of each command.



# 6.0 Timings

The timing of BSY and DRQ in Status Register are shown in the table below.

**Table 11: Timeout Values**

| FUNCTION              | INTERVAL                          | START  | STOP  | TIMEOUT |
|-----------------------|-----------------------------------|--|---|---------|
| Power On and COMRESET | Device Ready After Power On       | COMRESET   | The Device sets BSY(=0) and RDY(=1) to the Status Register and requests to send the Register FIS to the Host. | 31 sec  |
| Software Reset        | Device Busy After Software Reset  | The Host asserts SRST(=1) to the Device Control Register and send the Register FIS to the Device.  | The Host Adapter sets BSY(=1) to the Status Register.   | 400 ns  |
|                       | Device Ready After Software Reset | The Host asserts SRST(=1) to the Device Control Register and send the Register FIS to the Device. Then the Host negates SRST(=0) to the Device Control Register and send the Register FIS to the Device. | The Device sets BSY(=0) and RDY(=1) to the Status Register and requests to send the Register FIS to the Host. | 31 sec  |

| FUNCTION            | INTERVAL  | START  | STOP  | TIMEOUT |
|---------------------|---|--|---|---------|
| COMRESET            | Device Ready After COMRESET                     | COMRESET Signal Asserted   | The Device sets BSY(=0) and RDY(=1) to the Status Register and requests to send the Register FIS to the Host.   | 31 sec  |
| Non-Data Command    | Device Busy After the register FIS For Command. | The host sets commands to Command Register and sends the Register FIS.               | The Host Adapter sets BSY(=1) to the Status Register.   | 400 ns  |
|                     | The Register FIS For Command Complete           | The Host Adapter sets BSY(=1) to the Status Register.                                | The Device sets the status of command to the Status Register and requests to send the Register FIS to the host. | 30 sec  |
| PIO Data In Command | Device Busy After the Register FIS For Command. | The Host sets commands to Command Register and sends the Register FIS to the Device. | The Host Adapter sets BSY(=1) to the Status Register.   | 400 ns  |
|                     | PIO SETUP FIS For Data Transfer In              | The Host Adapter sets BSY(=1) to the Status Register.                                | The Device sets BSY(=0) and DRQ(=1) to the Status Register and requests to send the PIO SETUP FIS to the Host.  | 30 sec  |
|                     | Device Busy After Data Transfer In              | The PIO SETUP FIS is transferred to the Host.  | The Host Adapter sets BSY(=1) to the Status Register.   | 400 ns  |

| FUNCTION                  | INTERVAL  | START  | STOP   | TIMEOUT |
|---------------------------|---|--|--|---------|
| PIO Data Out Command      | Device Busy After the Register FIS For Command. | The Host sets commands to Command Register and sends the Register FIS to the Device. | The Host Adapter sets BSY(=1) to the Status Register.  | 400 ns  |
|                           | Device Busy After Data Transfer Out             | The Host sends the Data FIS to the Device.   | The Host Adapter sets BSY(=1) to the Status Register.  | 400 ns  |
|                           | PIO SETUP FIS For Data Transfer Out             | The Host Adapter sets BSY(=1) to the Status Register.                                | The Device sets BSY(=0) and DRQ(=1) to the Status Register and requests to send the PIO SETUP FIS to the host. | 30 sec  |
| DMA Data Transfer Command | Device Busy After the Register FIS For Command. | The Host sets commands to Command Register and sends the Register FIS.               | The Host Adapter sets BSY(=1) to the Status Register.  | 400 ns  |

Command category is referred to in section 11.0, "Command protocol" on page 105.

The abbreviations "ns", "µs", "ms," and "sec" mean nanoseconds, microseconds, milliseconds, and seconds, respectively.

It is recommended that the host system executes Soft reset and then retries to issue the command if the host system timeout would occur for the device.

If the host detects a time-out while waiting for a response from the device, we recommend that the host system execute a Soft reset and then retry the command.

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