Are You Ready for CE-ATA?

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Introduction

CE-ATA*, the newest hard disk drive interface, is the solution to IO bound host designs. This new interface, with a total of 12 wires (4 bit data bus), supports hard disk drives up to 144,000 TERABYTES! CE-ATA is perfect for multi-media players, cell phones and other handheld devices. With a 26MB/sec (4 bit data bus) maximum transfer rate, the interface can support all applications.

If you're looking for a large amount of storage in a small space with a simple interface, look no further. Read on to see how you can join the CE-ATA bandwagon and have up to 8GB of storage in your handheld device.

MMC roots

The CE-ATA hardware interface gets its roots from the MMC** version 4.0 specification. The MMC System Summary, found at http://www.mmca.org/tech/MMCA_System_summaryV41.pdf, offers a clear explanation of MMC.

The MMC interface consists of Power, Ground, Data (DAT) (either 1, 4 or 8 bits), Command (CMD), and Clock (CLK) lines. In general, MMC has a bus architecture. However, version 4.1, called the high speed version (up to 52MHz clock), defines a one card per bus limitation. The CE-ATA specification does not support the shared bus approach. Commands are transferred from the host to the device serially over the CMD line in sync with CLK transitions. Responses to commands are transferred from the device to the host over the CMD line in sync with CLK transitions. Data is transferred from either the host or the device over the DAT line(s) in sync with CLK transitions. Data widths of 1, 4 or 8 bits are supported by the specification, however the Hitachi Microdrive® 3K8 supports only 1 or 4 bit data busses. The width of the Data bus is negotiated during the initialization phase of host-device communication.

The very basic MMC commands are supplemented with a new ATA command subset that permits random read/write access to the storage device. Issuing a single command can permit data to be transferred from 4 thousand bytes to 33 megabytes, to or from the host.

CE-ATA command protocol

CE-ATA uses these MMC commands: CMD0 (GO_IDLE_STATE), CMD12 (STOP_TRANSMISSION), CMD39 (FAST_IO), CMD60 (RW_MILTIPLE_REGISTER), CMD61 (RW_MULITPLE_BLOCK). The latter two commands are detailed in the CE-ATA specification and the others are defined by the MMC specification.

CMD60 permits the entire ATA Task File (16 bytes) to be transferred to the device with a single command sequence, rather than the conventional method of a register at a time. This speeds up the ATA command setup considerably.

The MMC specification defines the protocol in detail which is beyond the scope of this document.

Connector and pin assignment

The Hitachi CE-ATA models of Microdrive 3K8 will use a 0.5mm pitch, 12 pin, ZIF connector for a flex circuit connection. The pin assignment table is shown in Figure 1.

Pin	Signal Name
1	Vss
2	DAT2
3	DAT3
4	Supply Voltage
5	CMD
6	Interface Voltage
7	CLK
8	Vss
9	DAT0
10	DAT1
11	Vss
12	Reserved

Figure 1: Connector pin assignment

Basic interface protocol

Each cycle of the clock (CLK) signal, directs one bit of information to transfer between the host and the device. The frequency may vary from zero to the maximum supported frequency (52MHz for the Microdrive 3K8).

A bi-directional command (CMD) signal, is used for commands and card initialization. The command signal operates in open drain mode during the initialization process and in push-pull mode during command transfers. Commands are sent from the host to the device and responses are sent from the device to the host.

The specification defines the data transfer to be up to 8 data bits. The Microdrive 3K8 supports 1 or 4 bits. The width of the data bus is defined as part of the initialization process. These lines are bi-directional and operate in push-pull mode at all times. During initialization, DAT0 is only used for transfer of data. More lines (4 or 8) can be configured by the host after initialization.

Note the lack of a RESET line. The card is expected to be able to detect the loss of power and reset itself. The host may reset the card by removing and applying Vss or by special command. After loss of power, the card will always power up into a defined state after power is re-applied.

Device initialization and communication

The MMC System Summary mentioned above also provides a well defined overview of the initialization and command/response process. Details are found in the MMC specification which can be purchased on the MMCA website without a membership (http://www.mmca.org/compliance/buy_spec/). This document defines the initialization procedure and command/response process to permit sending ATA commands to the device.

Sample data flow

The CE-ATA specification provides the detail on how to use the MMC primitive command/response protocol to configure the ATA registers (with one command sequence) and execute ATA Read and Write commands from the device. The CE-ATA organization has implemented a reduced ATA command set to simplify the software required in the host and in the device.

The Read_Write_Multiple_Register command permits writing all 7 ATA registers at one time, reducing the overhead of single register addressing. Similarly, the Read_Write_Multiple_Block command permits reading a single sector or multiple sectors of data with a single command.

This is a typical data transfer flow after the initialization process:

A: Host to setup ATA task file in memory to prepare for transfer to device of the ATA command and parameters.

B: Host sends RW_MULITPLE_REGISTER command and gets R1 Response from device over CMD line.

C: Host transfers ATA Task file over DATA lines to device.

D: Host sends RW_MULTIPLE_BLOCK command and gets R1 Response from device over CMD line.

E: Host transfers data to be written OR device transfers data read over DATA lines.

F: When all blocks of DATA are transferred, the device will send Command Completion Signal on CMD line (if not disabled).

G: Host can then read the device status using either RW_MULTIPLE_REGISTER command or FAST_IO command to verify that the data was written/read to/from disk error free.

Summary

The purpose of this paper is to whet your appetite to implement CE-ATA in your consumer electronic device and to illustrate the simplicity of reading and writing data to a hard disk drive.

The file structure is not discussed since that is primarily Operating System (OS) dependant. Using an embedded Windows, Linux or roll-your-own operating system will define the file system required. The MMC summary provides an introduction to file formats with and without a Partition Table. For more about disk file formats, read the Hitachi whitepaper titled An Introduction to FAT File Systems, available at www.hitachigst.com.

* More information on CE-ATA standards can be found at: www.ce-ata.org

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