



S31L-9327-03

OEM HARD DISK DRIVE SPECIFICATIONS

for

DMDM - 10340 / 10170 (340 MB / 170 MB)

IBM microdrive with CF+ Type II Interface

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1.0 General

This document describes the specifications of the following IBM microdrives with CF+™ Type II interface:

- DMDM-10170 (170 MB)
- DMDM-10340 (340 MB)

Note: The specifications are subject to change without notice.

1.1 References

- ANSI ATA/ATAPI-4 working draft T13 1153D revision 18
- PC Card Standard March 1997 - volume 2: Electrical Specification
- PC Card Standard March 1997 - volume 4: Metaformat specification
- PC Card Standard March 1997 - volume 8: PC Card ATA Specification
- CompactFlash Specification Revision 1.3

1.2 Glossary

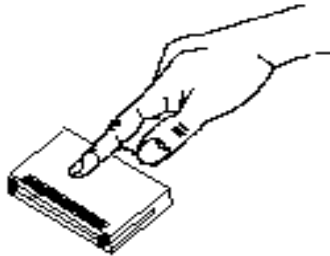
<i>Word</i>	<i>Meaning</i>
Kbpi	1 000 Bit Per Inch
Mbps	1 000 000 Bit per second
MB	1 000 000 bytes
KB	1 000 bytes
32 KB	32 x 1 024 bytes
64 KB	64 x 1 024 bytes
Mb/sq.in	1 000 000 bits per square inch
drive	DMDM-10340/10170
microdrive	DMDM-10340/10170
MLC	Machine Level Control
TBD	To Be Defined

1.3 General Caution

- Do not apply pressing force onto the top or bottom surface of microdrive. (See Figure 1. on page 2).
- Do not cover the breathing hole on the top cover (See Figure 2. on page 2).
- Do not touch the interface connector pins and the surface of printed circuit board.
- The microdrive can be easily damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

1.3.1 Caution of Handling

DO NOT PRESS!



**PRESSING DRIVE WILL
RESULT LOSS OF DATA**

Figure 1. Handling of DMDM-10340/10170

**DO NOT COVER
THIS HOLE**



**COVERING THIS HOLE WILL
RESULT LOSS OF DATA**

Figure 2. Breathing hole of DMDM-10340/10170

2.0 General Features

- **CF+ Type II Card Compliance**
- **340MB / 170MB formatted capacity**
- **GMR head**
- **512 bytes/sector**
- **CF+ Interface**
- **Integrated controller**
- **No-ID recording format**
- **PRML channel**
- **Multi Zone Recording**
- **On The Fly correction : 12 Bytes/sector**
- **128KB Buffer for Read and Write**
- **Host data transfer speed up to 5.2 MB/sec**
- **Media data transfer rate 45.2 (outer zone) - 30.1 (inner zone) Mbit/sec**
- **Average seek time 15 ms for read**
- **Closed-loop actuator servo (Embedded Sector Servo)**
- **True Track servo**
- **Rotary voice coil motor actuator**
- **Load / Unload mechanism**
- **Mechanical Latch**
- **Adaptive power save control (0.73 Watt Performance Idle average)**
- **0.16 sec Power on to ready**
- **Shock**
 - **Non-operating : 1000 G / 1 ms**
 - **Operating : 150 G / 2 ms**

Part 1. Functional Specifications

3.0 Drive Characteristics

This chapter provides the characteristics of the drives.

3.1 Logical Drive Format

The customer usable data capacity is as shown below.

Descriptions	DMDM-10170	DMDM-10340
Logical Head Number	16	16
Logical Sectors/Track	63	63
Logical Cylinder Number	344	695
Logical Sector Size	512	512
Total Customer Usable Data Sectors	346,752	701,568
Total Customer Usable Data Bytes	170 MB 177,537,024	340 MB 358,686,720

Figure 3. Drive Parameter

3.2 Data Sheet

Media transfer rate [Mb/sec]	30.1 - 45.2
Interface transfer rate [MB/sec]	5.2 MB/sec Max
Data buffer size [KB]	128 KB (Read / Write)
Rotational speed [RPM]	4500
Average latency [msec]	6.7
Recording density [Kbpi]	265.1 (Max)
Track density [Ktpi]	19
Areal density [Gb/sq.in.]	5.04 (Max)
Number of zone	8
Number of disks	1
Number of heads	2
Servo design method	Embedded sector servo

Figure 4. Data Sheet

3.3 Performance Characteristics

File performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
 - Seek Time
 - Latency
- Data Transfer Speed
- Buffering Operation

Note: All the above parameters contribute to a file performance. There are other parameters which contribute to the performance on the actual system. This specification tries to define the essential file characteristics, not the system throughput which is dependent on the system and the application.

The following table gives a typical value of each parameter. The detail descriptions are followed in the next sections.

Function	Typical
Average Random Seek Time For Read	15 msec
Average Random Seek Time For Write	17 msec
Rotational Speed	4500 rpm
Power On To Ready	1.0 sec
Command Overhead	1.0 msec
Disk-Buffer Data Transfer	45.2 - 30.1 Mbit/sec
Buffer-Host Data Transfer	5.2 MB/sec

Figure 5. Performance Parameter

3.3.1 Command Processing

Command overhead time is defined as the total time from when the command is received by the drive to the start of motion of the actuator.

3.3.2 Average Seek Time (Including Settling)

Command Type	Typical	Max
Read	15 msec	17 msec
Write	17 msec	19 msec

Figure 6. Mechanical Positioning Performance

'Typical' and 'Max' are given throughout the performance specification by;

- Typical** Average of the drive population tested at nominal environmental and voltage conditions.
- Max** Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See 5.1, "Environment" on page 13 and 5.2, "DC Power Requirements" on page 15)

The seek time is measured from the start of motion of the actuator to the timing of a reliable read or write operation may be started. Reliable read or write implies that error correction/recovery is not employed to correct for arrival problems. The Average Seek Time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\text{max}} (\text{max} + 1 - n) (T_{n.in} + T_{n.out})}{(\text{max} + 1) (\text{max})}$$

Where:

- max = Maximum Seek Length
- n = Seek Length (1 to max)
- T_{n.in} = Inward measured seek time for a n track seek
- T_{n.out} = Outward measured seek time for a n track seek

3.3.3 Single Track Seek Time

Function	Typical	Max
Read	2 msec	3 msec
Write	3 msec	4 msec

Figure 7. Single Track Seek Time

Single track seek is measured as the average of one (1) single track seek from every track in both directions (inward and outward).

3.3.4 Full Stroke Seek Time

Function	Typical	Max
Read	20 msec	23 msec
Write	22 msec	25 msec

Figure 8. Full Stroke Seek Time

Full stroke seek is measured as the average of 1000 full stroke seeks.

3.3.5 Average Latency

RPM	Time for a revolution	Average Latency
4500	13.3 msec	6.7 msec

Figure 9. Latency Time

3.3.6 Operating Modes.

Operating mode	Description
Spin Up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Performance idle	The device is capable of responding immediately to media access requests. All electronic components remain powered and full frequency servo remains operational.
Active idle	Not used.
Low power idle	Head is unloaded on the parking position. Spindle motor is rotating at full speed.
Standby	The device interface is capable of accepting commands. Spindle motor is stopped. All circuitry except host interface are in power saving mode. The execution of commands is delayed until spindle becomes ready.
Sleep	Same as Standby.

Figure 10. Operating Mode

3.3.6.1 Mode Transition Time.

From	To	Transition Time
Power On	Standby	0.16 sec typ, 0.2 sec max.
Standby	Idle	1.5 sec typ, 1.8 sec max.

Figure 11. Mode Transition Time

3.3.6.2 Operating mode at power on

The device goes to Standby mode after Power On or Hard Reset as an initial state.

3.3.6.3 Adaptive power save control

The transition timing from Performance Idle to Standby is adaptively and automatically controlled with the access pattern of the host system.

4.0 Data Integrity

4.1 Data Loss by Power Off

- The drive retains recorded data under all non-write operations.
- No more than one sector can be lost by power down during write operation while write cache is disabled.
- Power off during write operation may make an incomplete sector which will report hard data error when read. The sector can be recovered by a re-write operation.
- Hard reset does not cause any data loss.

4.2 Write Cache

Manufacturing ship default is Write Cache disable.

Write Cache can be enabled or disabled by Set Features command. Refer to 7.4.18, "Set Features - EFh" on page 64

- Power off while write cache is enabled may cause loss of data which are remaining in the cache and have not been flushed onto the disk media.
- This means that there is a possibility that power off even after write command completion may cause loss of data.
- There are ways to check if all data in the write cache have been flushed onto the disk. Checking just before power off is recommended to prevent data loss.
 - To confirm successful completion of Software Reset.
 - To confirm successful completion of Flush Cache command.
 - To confirm successful completion of Standby command.
 - To confirm successful completion of Standby Immediate command.

Note: For Power Off Sequence, refer to 5.3.4, "Load/Unload" on page 18.
Write Cache is disabled as ship default.

4.3 Equipment Status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following condition is satisfied:

- Self-check of drive is complete.

Appropriate error status is made available to the host system if any of the following conditions occur after the drive has once become ready:

- Spindle speed outside requirements for reliable operation.
- Occurrence of a WRITE FAULT condition.

4.4 WRITE Safety

The drive ensures that the data is written onto the disk media properly. Following conditions are monitored during a write operation. When one of those conditions exceeds the criteria, the write operation is terminated and automatic retry sequence will be invoked.

- Head off track
- External shock
- Low supply voltage
- Spindle speed tolerance
- Head open/short

4.5 Data buffer test

The data buffer is tested at Power-on-reset and when a drive self-test is requested by the host. The tests consist of write/read '00'x and 'ff'x pattern on all buffer.

4.6 Error Recovery

Errors occurring on the drive are handled by the error recovery procedure.

Errors that are uncorrectable after application of the error recovery procedures are reported to the host system as non-recoverable errors.

4.7 Automatic Reallocation

The sectors those show some errors may be reallocated automatically when specific conditions are met. The drive does not report for auto-reallocation to the host system. The conditions for auto-reallocation are described below.

4.7.1 Non Recovered Write Errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation has failed.

4.7.2 Non Recovered Read Errors

When a read operation has failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered locations specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

4.7.3 Recovered Read Errors

When a read operation for a sector failed once and then recovered at the specific ERP step, this sector is reallocated automatically. A media verification sequence may be run prior to the reallocation according to the pre-defined conditions.

5.0 Specification

5.1 Environment

5.1.1 Temperature and Humidity

Operating Conditions	
Temperature	5 to 55[×C] (See note)
Relative Humidity	8 to 90 [%RH] non-condensing
Maximum Wet Bulb Temperature	29.4[×C] non-condensing
Maximum Temperature Gradient	20[×C / Hour]
Altitude	-300 to 3000 [m]
Non-Operating Conditions	
Temperature	-40 to 65[×C]
Relative Humidity	5 to 95 [%RH] non-condensing
Maximum Wet Bulb Temperature	40[×C] non-condensing
Maximum Temperature Gradient	20[×C / Hour]
Altitude	-300 to 12,000 [m]
Note: The system has to provide sufficient ventilation to maintain a surface temperature below 60[×C]. Non-operating condition should not continue beyond one year.	

Figure 12. Environmental Condition

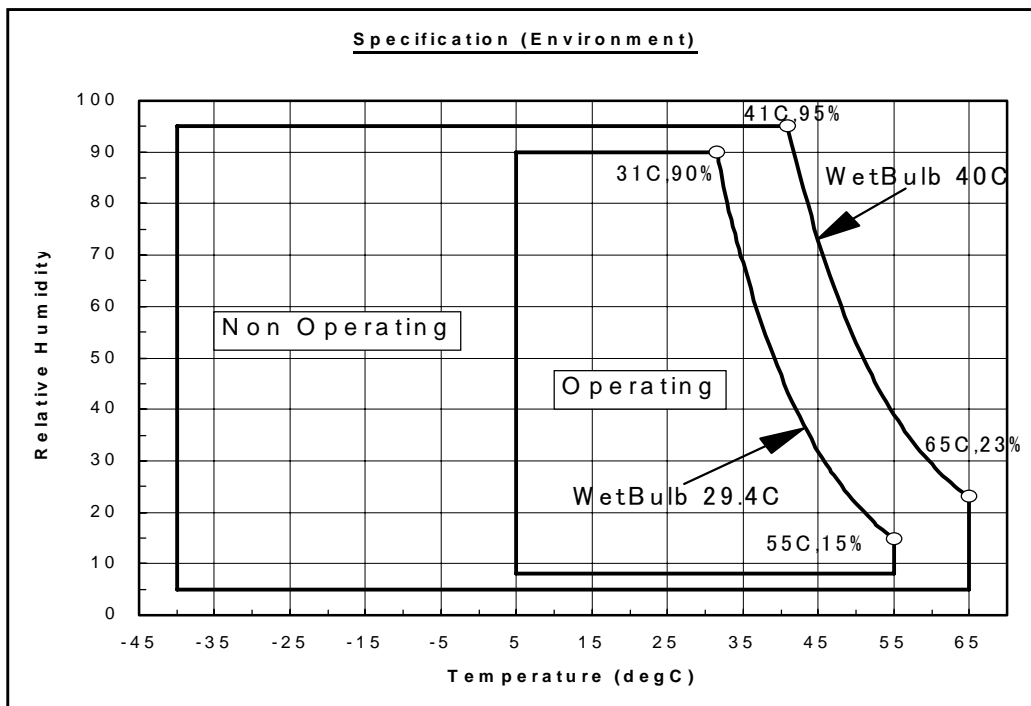


Figure 13. Temperature and Humidity Limitation

5.1.2 Magnetic Fields

The disk drive will withstand radiation & conductive noise within the limits shown below.

5.1.2.1 Radiation Noise

The disk drive shall work without degradation of the soft error rate under the following Magnetic Flux Density Limits at the enclosure surface.

Frequency (KHz)	Limits (Gauss rms)
0 - 60	5.0
61 - 100	2.5
101 - 200	1.0
201 - 400	0.5

Figure 14. Magnetic Flux Density Limits

5.1.2.2 Conductive Noise

The disk drive shall work without degradation of the soft error rate, with an AC current of up to 45 mA(p-p), in the frequency range from DC to 20 MHz, injected through any two of the mounting screw holes of the drive via 50ohm resistor.

5.2 DC Power Requirements

Connection to the product should be made in isolated secondary circuits (SELV). The voltage specifications are applied at the power connector of the drive

DMDM-10340/10170 supports both 3.3V and 5V power supply, and the voltage is automatically detected by the drive..

Item	+3.3V power supply case	+5V power supply case	Notes
Nominal Supply	+3.3 Volt	+5 Volt	*0
Power Supply Ripple (0- 20Mhz)	70 mv p-p max	100 mv p-p max	*1
Tolerance	+/-5%	+/-5%	*2
Supply Current	Pop.Mean (Nominal Condition)	Pop.Mean (Nominal Condition)	
Performance Idle average	230 mA RMS typical (0.8 W)	260 mA RMS typical (1.3 W)	*3
Low power Idle average	210 mA RMS typical (0.7 W)	240 mA RMS typical (1.2 W)	
Read average	280 mA RMS typical (0.9 W)	320 mA RMS typical (1.6 W)	*4
Write average	300 mA RMS typical (1.0 W)	330 mA RMS typical (1.7 W)	
Seek average	270 mA RMS typical (0.9 W)	310 mA RMS typical (1.5 W)	*5
Standby	65 mA RMS typical (0.2 W)	80 mA RMS typical (0.4 W)	
Start up (maximum RMS in 10 ms windows)	260 mA RMS typical (0.9 W)	280 mA RMS typical (1.4 W)	*6
Supply Rise Time	0 - 100 ms	0 - 100 ms	

Figure 15. Power Requirement

Notes :

- (*0) Current limiter less than 10A is recommended in user application to keep safe.
- (*1) The maximum fixed disk ripple is measured at 3.3 / 5V input of the drive.
- (*2) The disk drive shall not incur damage for an over voltage condition of +25% (maximum duration of 20 ms) on the 3.3 / 5 volt nominal supply.
- (*3) The idle current is specified at an inner track.
- (*4) The read/write current is specified based on three operations of 63 sector read/write per 100 msec.
- (*5) The seek average current is specified based on three operations per 100 msec.
- (*6) The typical current wave form at start up is shown in Figure 16. on page 16.

5.2.1 Start Up Current

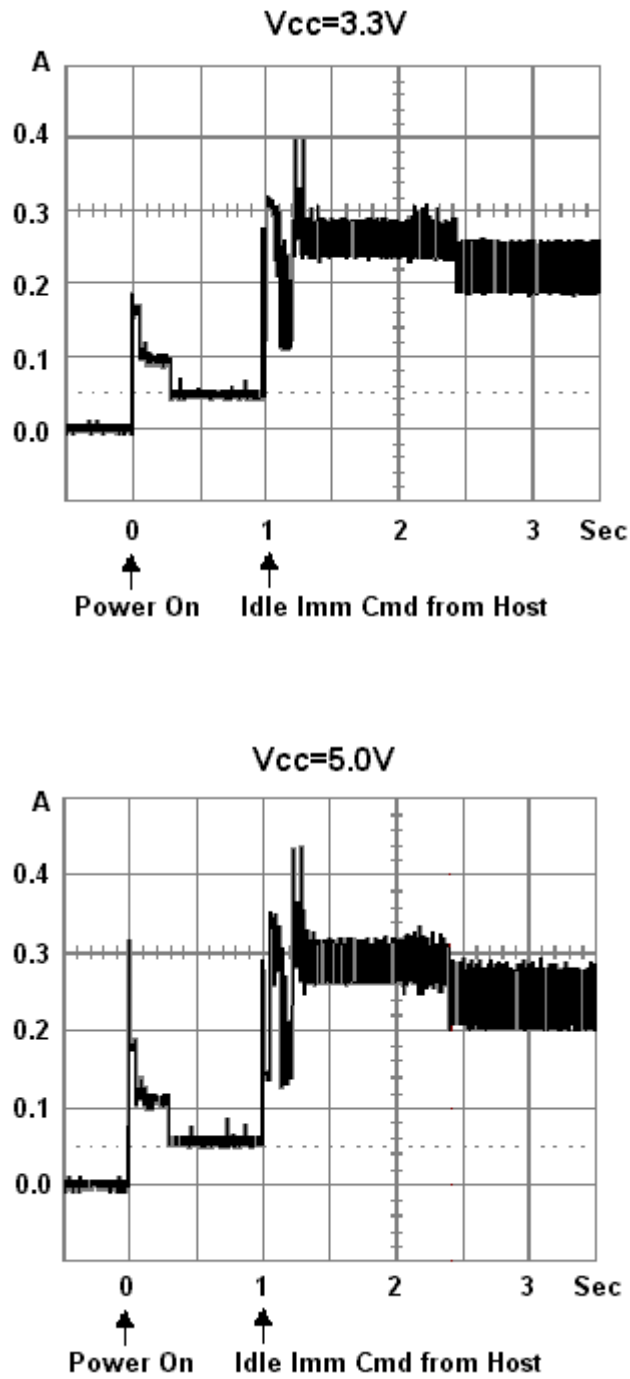


Figure 16. Typical current wave form at start up.

5.3 Reliability

5.3.1 Data Reliability

- Probability of not recovering data 1 in 10^{13} bits read
- ECC On-The-Fly correction, performed as a part of read channel function, recovers up to 12 symbols of error in 1 sector. (1 symbol is 8 bits.)

5.3.2 Drive Usage Condition

The drive is designed to be used under the following conditions.

- Within specifications of Shock, Vibration, Temperature, Humidity, Altitude, and Magnetic Field.
- ESD protective handling.
- Kept in Antistatic Plastic Case.
- Without covering breathing hole on microdrive surface. (Refer to Figure 2. on page 2)
- Without pressing microdrive surface. (Refer to Figure 1. on page 2)
- Less than 140 power-on hours per month.
- Seeking/Writing/Reading operation be less than 20% of power-on hours.
- The power requirements be satisfied. (Refer to 5.2 on page 15)
- Interface connector firmly mated.
- Power off sequence according to 5.3.4.2, "Required Power-Off Sequence" on page 18.

Service life of DMDM-10340/10170 is approximately 5 years or 8400 power-on hours, whichever comes first.¹

Actual product life and failure rate depend on duty cycle and environmental conditions. Consult your IBM representative for reliability estimate if atypical operating conditions are anticipated.

5.3.3 Preventive Maintenance

None.

1. This does not represent any warranty nor warranty period. Applicable warranty and warranty period are covered by purchase agreement.

5.3.4 Load/Unload

The product supports a minimum of 300,000 normal load/unloads.

Load/unload is a functional mechanism of the HDD. It is controlled by the drive microcode. Specifically, unloading of the heads is invoked by the commands:

- Soft Reset
- Standby
- Standby Immediate

Load/unload is also invoked as one of the idle modes of the drive.

The specified start/stop life of the product assumes that load/unload is operated normally, not in emergency mode.

5.3.4.1 Emergency Unload

When HDD power is interrupted while the heads are still loaded, the microcode cannot operate and the normal 5v or 3.3v power is unavailable to unload the heads. In this case, normal unload is not possible, so the heads are unloaded by routing the back-EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case, and the unload process is inherently less controllable without a normal seek current profile.

Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

DMDM-10340/10170 supports a minimum of 20,000 emergency unloads.

5.3.4.2 Required Power-Off Sequence

The required sequence for removing power from DMDM-10340/10170 is:

- Step 1: Issue one of the following commands.
 - Soft Reset
 - Standby
 - Standby Immediate

Note: Flush Cache command is insufficient for power off sequence, because the command does not invoke Unload.

- Step 2: Wait until Command Complete Status is returned.

In typical case, it takes 350ms for the command completion, however, command time out value needs to be 30sec considering error recovery time.

- Step 3: Terminate power to HDD.

This power-down sequence should be followed for entry into any system power-down state, or system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios such as battery removal during operation.

5.3.4.3 Power Switch Design Considerations

In systems that use DMDM-10340/10170 consideration should be given to the design of the system power switch.

IBM recommends that the switch operate under control of system microcode, as opposed to being 'hard wired'. The same recommendation is made for 'cover-close' switches. When a hard wired switch is turned off, emergency unload occurs, as well as the problems cited in 4.1, "Data Loss by Power Off" on page 11 and 4.2, "Write Cache" on page 11.

5.3.4.4 Test Considerations

Start/stop testing is classically performed to verify head/disk durability. In the case of DMDM-10340/10170 the heads do not land on the disk, so this type of test should be viewed as a test of the load/unload function.

Start/Stop testing should be done by commands through the interface, Not by power cycling the drive. Simple power cycling of DMDM-10340/10170 invokes the emergency unload mechanism, and subjects the HDD to non-typical mechanical stress.

Power cycling testing may be required to test the boot-up function of the system. In this case IBM recommends that the power-off portion of the cycle contain the sequence specified in 5.3.4.2, "Required Power-Off Sequence" on page 18. Again, if this is not done, the emergency unload function is invoked and non-typical stress results.

5.4 Mechanical Specifications

5.4.1 Mechanical Dimensions and Weight

Mechanical Dimension of DMDM-10340/10170 complies with CompactFlash Specification Revision 1.3 released by CompactFlash Association..

	DMDM-10170 / DMDM-10340
Height (mm)	5.0 +0.0 / -0.1
Width (mm)	42.80 ± 0.101
Length (mm)	36.40 ± 0.15
Weight (gram)	16 Max

Figure 17. Physical Dimension and Weight

5.4.2 Mechanical Outline

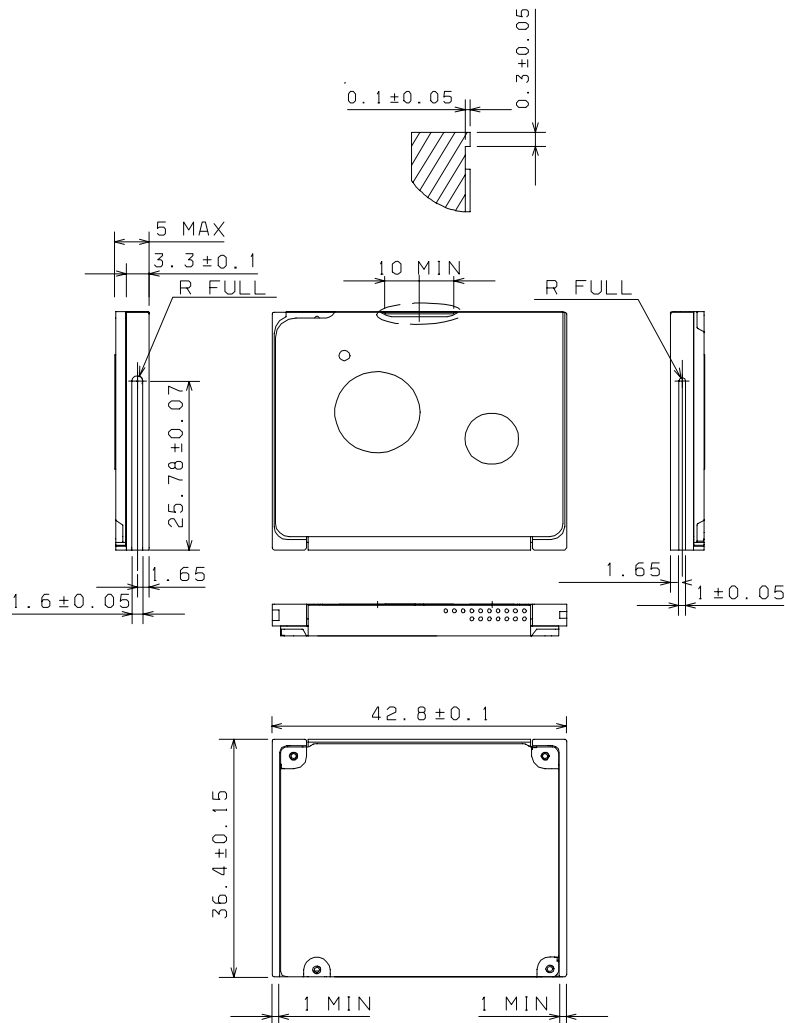


Figure 18. Mechanical Outline of DMDM-10340/10170

5.4.3 Interface Connector

Interface connector of DMDM-10340/10170 complies with CompactFlash™ Specification Revision 1.3.

5.4.4 Mounting Orientation

The drive will operate in all axes (6 directions).

The drive will operate within the specified error rates when tilted ± 5 degree from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted.

Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The system is responsible for mounting the drive securely enough to prevent excessive motion or vibration of the drive at seek operation or spindle rotation with adequate method.

Vibration test and shock test are to be conducted by mounting the drive to test table using a special fixture.

5.4.5 Head Load/Unload Mechanism

Head Load/Unload mechanism is equipped to protect data on the disk from any damage during shipping, movement or storage. Upon power down, the mechanism will secure the heads at unload position automatically, and upon power on, the heads are loaded automatically.

5.5 Vibration and Shock

All vibration and shock measurements in this section shall be for the disk drive without the mounting attachments for the systems. The input level shall be applied to the normal drive mounting points.

5.5.1 Operating Vibration

The disk drive will operate without a hard error while being subjected to the following vibration levels.

5.5.1.1 Random Vibration

The measurements are carried out with vibration test level 0.67G RMS (Root Mean Square) during 30 minutes of random vibration using the power spectrum density (PSD) as follows.

Random vibration PSD profile Break point

5 Hz	2.0 x E 5	g ² /Hz
17 Hz	1.1 x E 3	
45 Hz	1.1 x E 3	
48 Hz	8.0 x E 3	
62 Hz	8.0 x E 3	
65 Hz	1.0 x E 3	
150 Hz	1.0 x E 3	
200 Hz	5.0 x E 4	
500 Hz	5.0 x E 4	

The specified levels are measured at the mounting points.

5.5.1.2 Swept Sine Vibration

- 1 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 2.0 oct/min sweep rate

5.5.2 Non-Operating Vibration

5.5.2.1 Random Vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with the time duration of 15 minutes per axis. The PSD levels for the test simulates the shipping and relocation environment which is shown below.

	Random Vibration PSD Profile Break points (Non-Operating)			
Hz	2.5	5	40	500
G ² /Hz	0.001	0.03	0.018	0.018

Figure 19. Random Vibration PSD Profile Break points (Non-Operating)

Overall RMS level of vibration is 3.01G (RMS).

5.5.2.2 Swept Sine Vibration

- 25.4mm (peak to peak) displacement, 5 to 10 to 5 Hz
- 5 G (zero to peak), 10 to 500 to 10 Hz sine wave
- 0.5 oct/min sweep rate

5.5.3 Operating Shock

The hard disk drive meets the following criteria while operating in the conditions described below.

The shock test consists of ten shock inputs in each axis and direction for a total of 60.

There must be a minimum 3 seconds delay between shock pulses. Soft errors and automatic retries are allowed during the test.

No data loss or permanent damage : 150G / 2msec half-sine shock pulse, or 10G / 11msec half-sine shock pulse

The input level shall be applied to the normal disk drive subsystem mounting points, as mounted in normal system use.

5.5.4 Non-Operating Shock

The disk drive must withstand with no damage or degradation of performance, a 120G half-sine wave shock pulse of 11 ms duration and a 1000G half-sine wave shock pulse of 1 ms duration on six sides when heads are parked. (When the power is not applied to the unit, the heads are automatically located on the parked position.)

All shocks shall be applied in each direction of the drive's three mutually perpendicular axes, one axis at a time. Input levels shall be measured at the frame of the disk drive.

5.6 Acoustics

5.6.1 Sound Power Level

The criteria of A-weighted sound power level is described below.

Measurements are to be taken in accordance with ISO 7779. The mean of 40 drives is to be less than the typical value. Each drive is to be less than the maximum value. Drives are to meet this requirement in both board down orientations.

A-weighted Sound Power (Bels)	Typical	Maximum
Idle	2.3	2.6
Operating	2.4	2.7

Background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive be located at 25 +/- 3mm height from the chamber floor. No sound absorbing material shall be used.

The acoustical characteristics of the disk drive are measured under the following conditions.

Idle mode :

Power on, disks spinning, track following, unit ready to receive and respond to control line commands.

Operating mode :

Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as shown below.

$$N_s = 0.4 / (T_t + T_1)$$

where:

N_s: Average seek rate in seeks/s.

T_t: Published seek time from one random track to another without including rotational latency.

T₁: Equivalent time, in seconds, for the drive to rotate by half a revolution.

5.6.2 Discrete Tone Penalty

Discrete tone penalties are added to the A-weighted sound power (L_w) with following formula only when determining compliance.

$$L_{wt(spec)} = L_w + 0.1P_t + 0.3 < 4.0 \text{ (Bels)}$$

where:

L_w : A-weighted sound power level.

P_t : Value of discrete tone penalty = dLt-6.0 (dBA)

dLt : Tone-to-noise ratio taken in accordance with ISO 7779. at each octave band.

5.7 Identification

5.7.1 Drive Label

A Drive Label is affixed covering three surfaces (top, rear and bottom) onto each IBM microdrive.

The label contains ;

- Model name
- Part number
- Maker name
- Country of origin
- Notification to users
- Agency approval marks
- Bar code of serial number
- IBM logo
- Capacity
- Product name
- Certification mark of CompactFlash Association

No additional requirements by customer are allowed, due to space limitation.

5.8 Electromagnetic Compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, shall meet the worldwide EMC requirements listed below.

IBM will provide technical support to assist users in complying with the EMC requirements.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).

5.8.1 CE Mark

The product is certified for compliance to EC directive 89/336/EEC. CE marking for the certification appears on the drive.

5.8.2 C-Tick Mark

The product complies with the following Australian EMC standard.

- Limits and methods of measurement of radio disturbance characteristics of information technology equipment, AS/NZS 3548:1995 Class B.

5.9 Safety

5.9.1 Underwriters Lab(UL) Approval

DMDM-10340/10170 complies with UL 1950.

5.9.2 Canadian Standards Authority(CSA) Approval

DMDM-10340/10170 complies with CSA C22.2, #950-M1995.

5.9.3 IEC Compliance

DMDM-10340/10170 complies with IEC 950.

5.9.3.1 German Safety Mark

DMDM-10340/10170 are approved by TUV on Test Requirement:

EN 60 950:1988/A1:1990/A2:1991.

5.9.4 Flammability

Printed Circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better except minor mechanical parts.

5.9.5 Secondary Circuit Protection

This product utilizes printed circuit wiring that must be protected against the possibility of sustained combustion due to circuit or component failure. Adequate secondary over current protection is the responsibility of the using system.

User must protect the drive from it's electrical short circuit problem. 500mA limit is required for safety purpose.

5.10 Packaging

Drives will be shipped in appropriate container.

Drives are shipped in ESD protective bags.

6.0 Electrical Interface Specifications

6.1 Cabling

The maximum cable length from the host system to the drive plus circuit pattern length in the host system shall not exceed 18 inches.

6.2 Interface Connector

Interface connector of DMDM-10340/10170 complies with CompactFlash Specification version 1.3 which was released by CompactFlash Association.

Figure 18. on page 20 shows the connector location.

6.2.1 Signal Definition

Signal definition of DMDM-10340/10170 complies with CompactFlash Specification version 1.3 released by CompactFlash Association.

6.3 Signal Description

For signal definition, refer to CompactFlash Specification version 1.3 released by CompactFlash Association.

6.4 Interface Logic Signal Levels

The interface logic signal has the following electrical specifications:

Symbol	Parameter	Condition	Min.		Typ.	Max.		Unit
			3.135V	4.75V		3.465V	5.25V	
VOH	"H" Output Voltage	IOH= 2.0mA(3.135V) 4.0mA(4.75V) IOH=3.5mA(3.135V) 7.0mA(4.75V)	READY, INPACK#, BVD1, BVD2 the other output	0.8Vcc		--		Volts
VOL	"L" Output Voltage	IOH=- 2.5mA(3.465V) 4.0mA(5.25V) IOH=- 4.0mA(3.465V) 7.0mA(5.25V)	READY, INPACK#, BVD1, BVD2 the other outputs	--		0.4		Volts
I _H	"H" Input Current	VIN=VCC	CE1#,CE2#, OE#,WE#, IORD#, IOWR#, REG#, CSEL, A10-A0 RESET BVD1, BVD2 D15 - D0	-1		1		uA
I _L	"L" Input Current	VIN= GND PC Card Mode	CE1#,CE2#, OE#,WE#, REG#, IORD#, IOWR#, CSEL	-14	-20	-90	-140	uA
			RESET	-7	-10	-45	-70	
			A10 - A0 D15 - D0	-1 -5		1 5		
		VIN= GND IDE Mode	CE1#,CE2#, IORD#, IOWR#, A10 - !0, RESET D15 - D0	-1		1		
		OE#,WE#, REG#, BVD1,BVD2, CSEL	-14	-20	-90	-140		

6.5 Attribute Memory Read Timing

Symbol	Item	Min.	Max.	Units
tc(R)	Read Cycle Time	300 (*1)		ns
ta(A)	Address Access Time		300 (*1)	ns
ta(CE)	Card Enable Access Time		300 (*1)	ns
ta(OE)	Output Enable Access Time		150	ns
tdis(CE)	Output Disable Time from CE		100	ns
tdis(OE)	Output Disable Time from OE		100	ns
ten(CE)	Output Enable Time from CE	5		ns
ten(OE)	Output Enable Time from OE	5		ns
tv(A)	Data Valid from Address Change	0		ns
tv(WT-OE)	WAIT# Valid from OE		35	ns
tw(WT)	WAIT# Pulse Width		1,500	ns
tv(WT)	Data Setup for WAIT# Released	0		ns

Notes:

*1: DMDM-10340/10170 asserts WAIT# at CIS read. Minimum cycle time and access time at CIS read are 350ns.

*2: The host must monitor WAIT#.

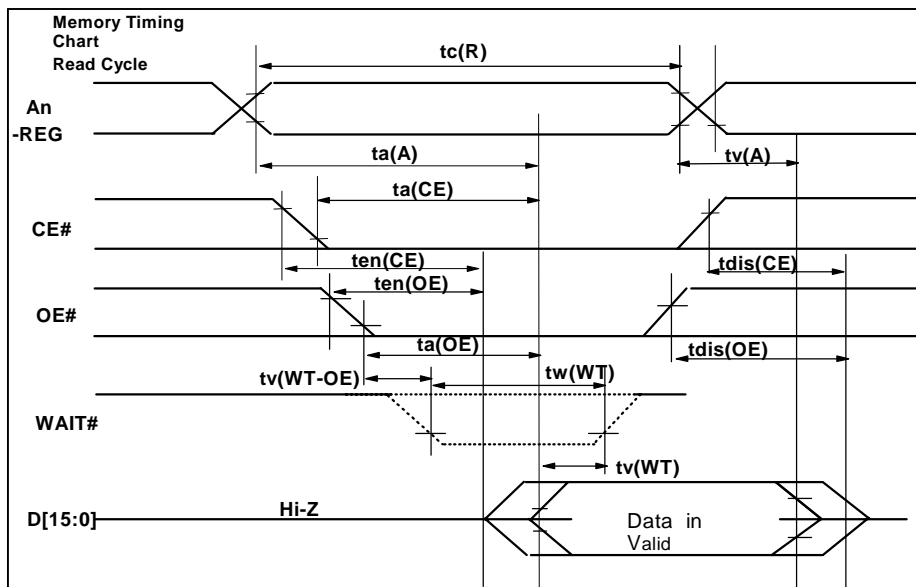
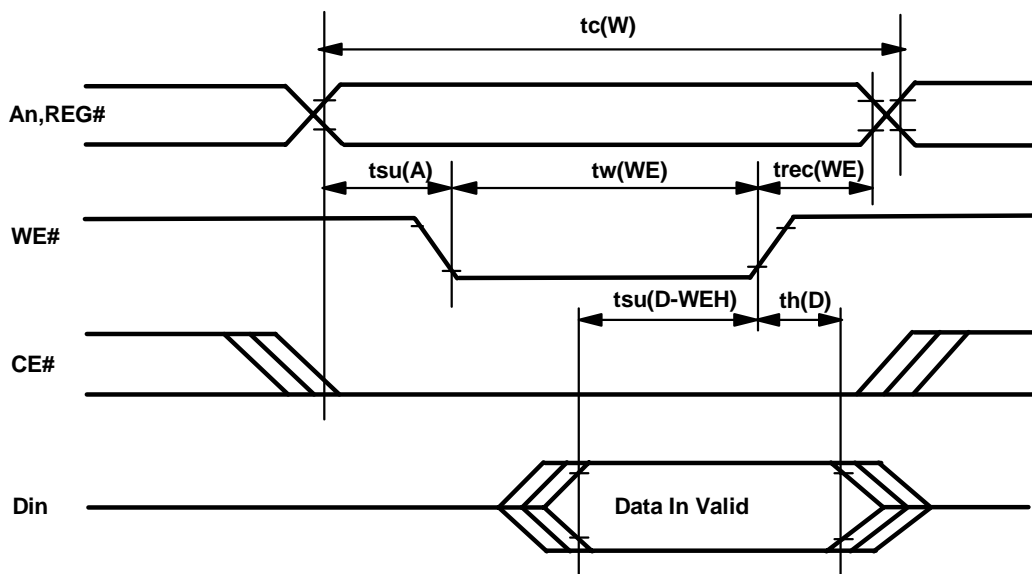


Figure 20. Attribute Memory Read Timing

6.6 Attribute Memory (Configuration Register) Write Timing

Symbol	Item	Min.	Max.	Units
$t_{c(W)}$	Write Cycle Time	250		ns
$t_{w(WE)}$	Write Pulse Width	150		ns
$t_{su(A)}$	Address Setup Time	30		ns
$t_{su(D-WEH)}$	Data Setup Time for WE="H"	80		ns
$t_{h(D)}$	Data Hold Time	30		ns
$t_{rec(WE)}$	Write Recovery Time	30		ns



OE# = "H"

Figure 21. Attribute Memory write Timing

6.7 Common Memory Read Timing

Symbol	Item	Min.	Max.	Units
taOE	Output Enable Access Time		125	ns
tdisCE	Output Disable Time from CE		100	ns
tsu(A)	Address Setup Time	30		ns
th(A)	Address Hold Time	20		ns
tsu(CE)	CE Setup before OE	5		ns
th(CE)	CE HOLD following OE	20		ns
tv(WT-OE)	Wait Delay Falling from OE		35	ns
tv(WT)	Data Setup for Wait Release	0		ns
tw(WT)	Wait Width Time		1,500 (*1)	ns

Notes:

*1: 350ns in the CF Specification 1.3 but it is planned to be changed as 3,000ns maximum in the next version.

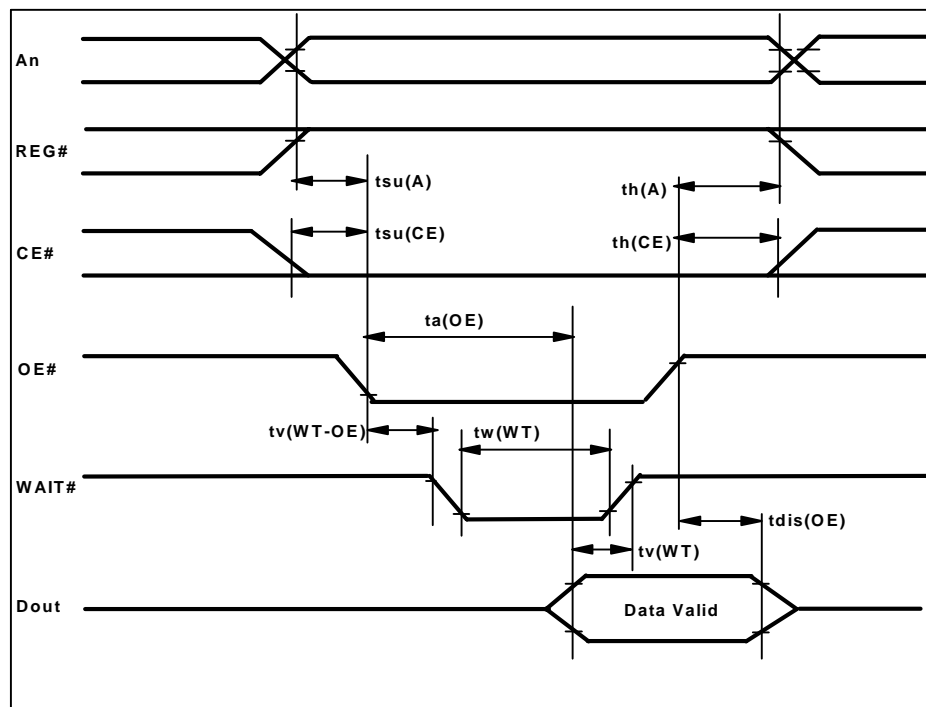


Figure 22. Common Memory Read Timing

6.8 Common Memory Write Timing

tsu(D-WEH)	Data Setup Time for WE="H"	80		ns
thD	Data Hold Time	30		ns
tw(WE)	Write Pulse Width	150		ns
tsu(A)	Address Setup Time	30		ns
tsu(CE)	CE Setup Time before WE	5		ns
trec(WE)	Write Recovery Time	30		ns
th(A)	Address Hold Time	20		ns
th(CE)	CE Hold following WE	20		ns
tv(WT-WE)	Wait Delay Falling from WE		35	ns
tv(WT)	WE High from Wait Release	0		ns
tw(WT)	Wait Width Time		1,500 (*1)	ns

Notes:

*1: 350ns in the CF Specification 1.3 but it is planned to be changed as 3,000ns maximum in the next version.

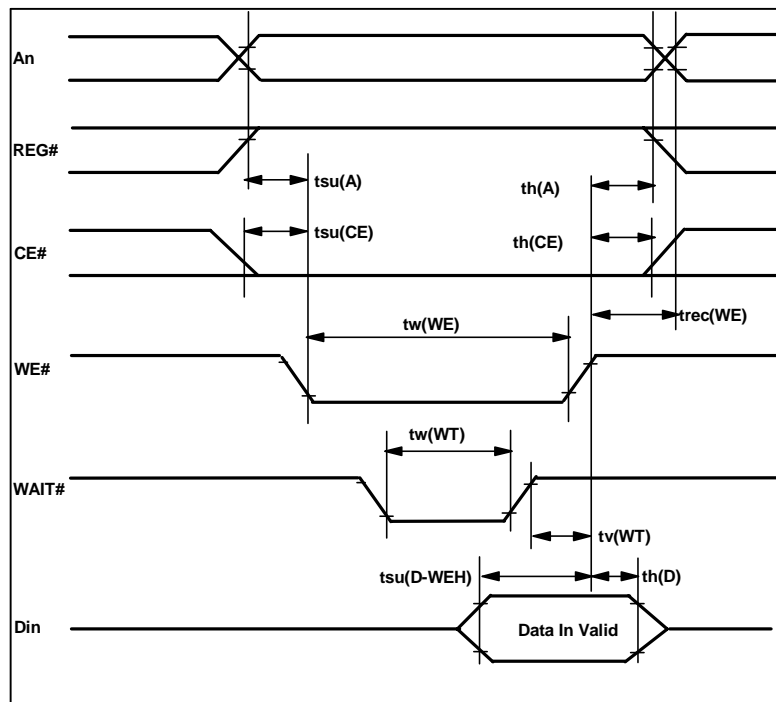


Figure 23. Common Memory Write Timing

6.9 I/O Input (Read) Timing

Symbol	Item	Min.	Max.	Units
td (IORD)	Data Delay after IORD		100	ns
th (IORD)	Data Hold following IORD	0		ns
tw (IORD)	IORD width Time	165		ns
tsu A (IORD)	Address Setup before IORD	70		ns
th A (IORD)	Address Hold following IORD	20		ns
tsu CE (IORD)	CE Setup before IORD	5		ns
th CE (IORD)	CE Hold following IORD	20		ns
tsu REG(IORD)	REG Setup before IORD	5		ns
th REG (IORD)	REG Hold following IORD	0		ns
tdf INPACK (IORD)	INPACK Delay Falling from IORD		45	ns
tdr INPACK (IORD)	INPACK Delay Rising from IORD		45	ns
tdf IOIS16(ADR)	IOIS16 Delay Falling from Address		35	ns
tdr IOIS16(ADR)	IOIS16 Delay Rising from Address		35	ns
tdf WT(IORD)	Wait Delay Falling from IORD		35	ns
tdr (WT)	Data Delay from Wait Rising		0	ns
tw (WT)	Wait Width Time		1,500 (*1)	ns

Notes:

*1: 350ns in the CF Specification 1.3 but it is planned to be changed as 3,000ns maximum in the next version.

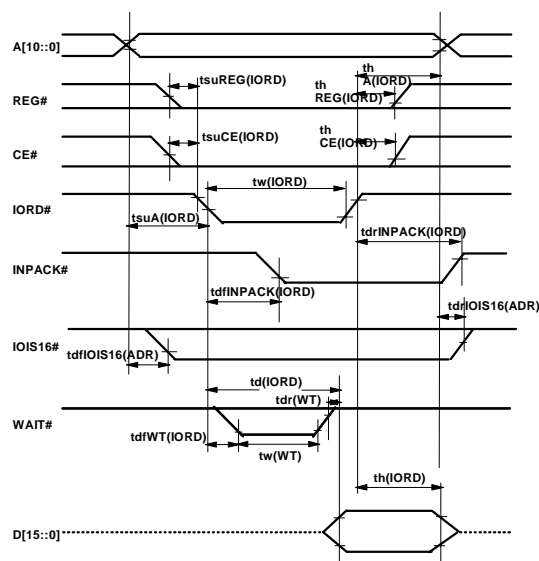


Figure 24. I/O Input (Read) Timing

6.10 I/O Output (Write) Timing

Symbol	Item	Min.	Max.	Units
td(IOWR)	Data Setup before IOWR	60		ns
th(IOWR)	Data Hold following IOWR	30		ns
tw(IOWR)	IOWR width Time	165		ns
tsuA(IOWR)	Address Setup before IOWR	70		ns
thA(IOWR)	Address Hold following IOWR	20		ns
tsuCE(IOWR)	CE Setup before IOWR	5		ns
thCE(IOWR)	CE Hold following IOWR	20		ns
tsu REG(IOWR)	REG Setup before IOWR	5		ns
th REG (IOWR)	REG Hold following IOWR	0		ns
tdf IOIS16 (ADR)	IOIS16 Delay following from Address		35	ns
tdr IOIS16 (ADR)	IOIS16 Delay rising from Address		35	ns
tdf WT(IOWR)	Wait Delay Falling from IOWR		35	ns
tdr IOWR(WT)	IOWR high from Wait high	0		ns
tw (WT)	Wait Width Time		1,500 (*1)	ns

Notes:

*1: 350ns in the CF Specification 1.3 but it is planned to be changed as 3,000ns maximum in the next version.

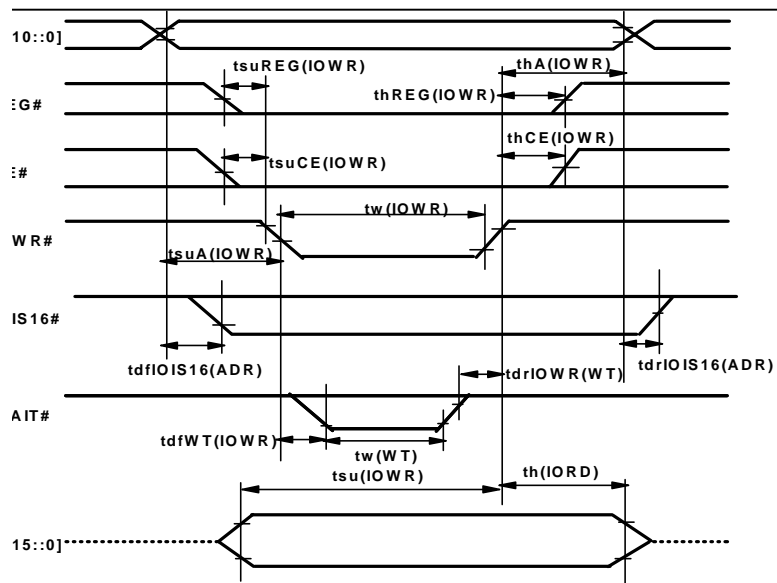


Figure 25. I/O Output (Write) Timing

6.11 True IDE Mode I/O Input (Read) Timing

Symbol	Item	Min.	Max.	Units
td (IORD)	Data Delay after IORD		100	ns
th (IORD)	Data Hold following IORD	0		ns
tw (IORD)	IORD width Time	165		ns
tsu A (IORD)	Address Setup before IORD	70		ns
th A (IORD)	Address Hold following IORD	20		ns
tsu CE (IORD)	CE Setup before IORD	5		ns
th CE (IORD)	CE Hold following IORD	20		ns
tdf IOIS16(ADR)	IOIS16 Delay Falling from Address		35	ns
tdr IOIS16(ADR)	IOIS16 Delay Rising from Address		35	ns

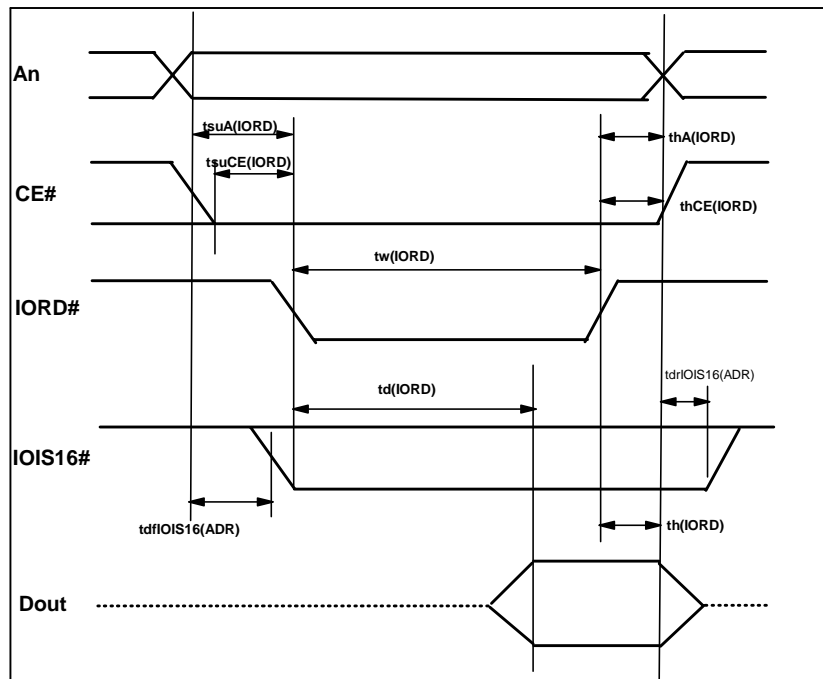


Figure 26. True IDE Mode I/O Input (Read) Timing

6.12 True IDE Mode I/O Output (Write) Timing

Symbol	Item	Min.	Max.	Units
td(IOWR)	Data Setup before IOWR	60		ns
th(IOWR)	Data Hold following IOWR	30		ns
tw(IOWR)	IOWR width Time	165		ns
tsuA(IOWR)	Address Setup before IOWR	70		ns
thA(IOWR)	Address Hold following IOWR	20		ns
tsuCE(IOWR)	CE Setup before IOWR	5		ns
thCE(IOWR)	CE Hold following IOWR	20		ns
tdf IOIS16 (ADR)	IOIS16 Delay following from Address		35	ns
tdr IOIS16 (ADR)	IOIS16 Delay rising from Address		35	ns

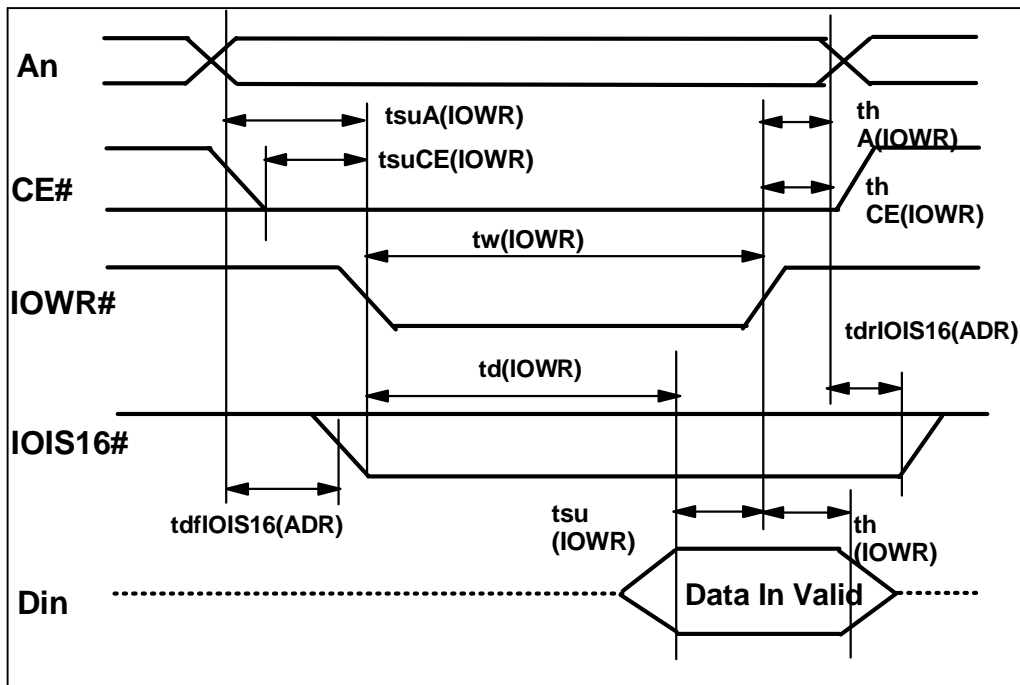


Figure 27. True IDE Mode I/O Output (Write) Timing

6.13 Power on/off Timing

Symbol	Item	Condition	Min.	Typ.	Max	Units
		$0\text{ V} \leq V_{cc} < 2\text{ V}$	0		V_{cc}	Volts
V_i (CE)	Card Enable signal level	$2\text{ V} \leq V_{cc} < V_{IH}$	$V_{cc} - 0.1$	V_{cc}	$V_{cc} + 0.1$	Volts
		$V_{IH} \leq V_{cc}$	V_{IH}		$V_{cc} + 0.1$	Volts
t_{su} (Vcc)	Card Enable Setup Time		20			ms
t_{su} (RESET)	RESET Setup Time		20			ms
t_{rec} (Vcc)	Card Enable Recovery Time		1			us
t_{pr}	Power rising Time	10% \rightarrow 90% of V_{cc}	0.1		100	ms
t_{pf}	Power falling Time	90% of $V_{cc} \rightarrow$ 10%	3		300	ms
t_w (RESET)	RESET puluse Width		10			us
t_h (Hi-zRESET)			1			ms
t_s (Hi-zRESET)			0			ms

Figure 28. Power On/Off Timing (1/2)

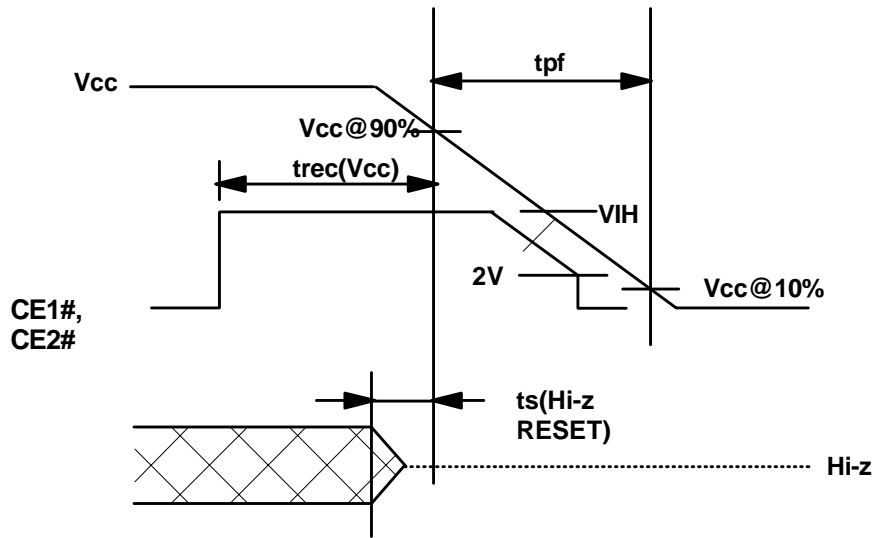
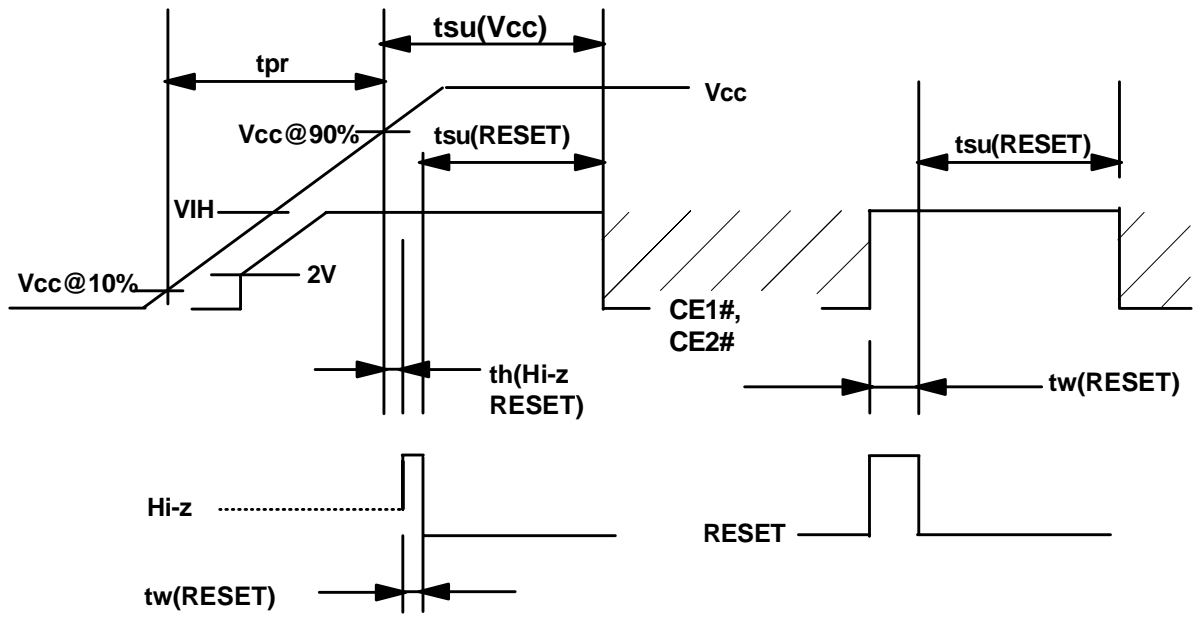


Figure 29. Power On/Off Timing (2/2)

Part 2. Interface Specifications

7.0 System Interface

7.1 PCMCIA Memory Spaces and Configuration Registers

There are two types of memory address space in the IBM microdrive: common memory and attribute memory. Common memory is the working address space used to map the memory arrays for storing data. It may be accessed by the host for memory read and write operations. The card permits both 8 and 16 bit accesses to all of its common memory addresses. Attribute memory is used for configuration information, and is limited to 8-bit wide accesses only at even addresses. The attribute memory space contains the CIS (Card Information Structure) and configuration registers. The IBM microdrive is identified by appropriate information in the CIS. The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system.

- CE 2	- CE 1	- REG	- OE	- WE	A 1 0	A 9	A8-A4	A 3	A 2	A 1	A 0	Selected space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8-bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8-bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16-bit D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8-bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8-bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16-bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Figure 30. Registers and memory space decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	Selected register
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Figure 31. Configuration registers decoding

7.2 Card Configuration Registers

The IBM microdrive has a set of configuration registers in attribute memory space. These registers are used to control the configurable characteristics of the card. The configurable characteristics include the electrical interface, I/O address space, interrupt request, and power requirements of the card. These registers also provide a method for accessing status information about the card. The information can be used to arbitrate between multiple-interrupt sources on the same interrupt request level. Address of the configuration registers are specified by the Configuration registers Base Address in the TPCC_RADR field of the Configuration Tuple and offset relative to the base address. For example, the Configuration and Status register can be located at offset 02h from the base address. The addresses of the card configuration registers should always be read from the CIS since these addresses may vary in future products.

7.2.1 Configuration Option Register (Offset 00h)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the IBM microdrive.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET: Soft Reset \bar{n} Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the card in the Reset state. Setting this bit to one (1) is equivalent to assertion of +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the card in the same unconfigured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using PCMCIA Soft Reset is considered a hard reset from the ATA point of view. An $\bar{i}ATA\bar{i}$ soft reset is issued through the Device Control Register.

LevIREQ: This bit is set to (1) when level mode Interrupt is selected, and zero (0) when pulse mode is selected. Set to zero (0) by. This bit is set to zero (0) by power-up and hardware reset. When the card is in Level Mode, the $\bar{n}IREQ$ pin is pulled up to Vcc on the card and asserted low to signal an interrupt. The interrupt is kept asserted until the host reads the card's status register, thereby resetting the interrupt indication and causing $\bar{n}IREQ$ to be deasserted. When the card is in pulse mode, the card signals an interrupt by the trailing edge of the negative pulse which width is at least 0.5 microseconds.

Conf5 \bar{n} Conf0: Configuration Index. This is set to zero (0) by power-up and hardware reset. It is used to select operation mode of the card as shown below. Conf5 and Conf4 are reserved and must be written as zero (0).

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Card Configuration Mode
0	0	0	0	0	0	Memory mapped
0	0	0	0	0	1	I/O mapped 16 contiguous registers at any 16-byte system decoded boundary
0	0	0	0	1	0	Primary I/O mapped, 1F0h \bar{n} 1F7h/3F6h \bar{n} 3F7h
0	0	0	0	1	1	Secondary I/O mapped, 170h \bar{n} 177h/376h \bar{n} 377h

7.2.2 Card Configuration Status Register (Offset 02h)

The Card Configuration and Status Register contains information about the card condition.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	-XP	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	-XP	0	PwrDwn	0	0

Changed: This bit indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, pin 46 (-STSCHG) is held low if the SigChg bit is a one (1) and the card is configured for the I/O interface.

SigChg: This bit serves as a gate for pin 46 (-STSCHG). If the card is configured for the I/O interface and this bit is zero (0), pin 46 (-STSCHG) is held high. If the card is configured for the I/O interface and both the Changed and SigChg bits are set to one (1), the card asserts pin 46 (-STSCHG) upon changes in the Changed bit.

IOis8: This bit is set to one (1) when the card is configured in 8-bit I/O mode as the host provides I/O cycles only with an 8-bit (D7-D0) data path.

-XE: Extended power enabled. When the host sets this bit to zero (0), the card enables extended power operations. When the host sets this field to one (1), the card disables extended power operations. When this field is read, the bit indicates the card's acceptance of extended power operations. If it is read as one (1), extended power operations are being disabled. If it is read as zero (0), the card can perform extended power operations. This bit is read as zero (0) after power-up and hardware reset. Identify Device information word 170 also has -XE bit for the same purpose. These -XE bits are always consistent. Extended power operations are defined as a command that requires the host's extended power capability. For the IBM microdrive, extended power operations includes any read, write and seek commands. Identify Device, Set Features (Enable Extended Power and Disable Extended Power), Request Sense and Execute Device Diagnostics are not extended power operations, i.e., these commands can be performed regardless of the setting in -XE bit.

PwrDwn: This bit indicates whether the host requires the card to be in the power saving or active mode. When the bit is one (1), the card enters power down mode, which is the same mode the card enters upon a completion of Sleep command. When the bit is zero (0), the card enters the active mode. The PCMCIA Rdy/-Bsy signal becomes BUSY when this bit is changed. Rdy/-Bsy will not become READY until the power state requested has been entered. The IBM microdrive automatically powers down when it is idle and powers back up when it receives a command. Duration of active mode to power down mode is variable as determined by the Adaptive Battery Life Extender 3 (ABLE-3) technology.

Int: This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the IEN bit in the Device Control Register, this bit is zero (0).

7.2.3 Pin Replacement Register (Offset 04h)

The Pin Replacement Register is used to provide the card status information about READY and WP.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	0	1	1	Rdy/-Bsy	0
Write	0	0	CRdy/-Bsy	0	0	0	MRdy/-Bsy	0

Crdy/-Bsy: This bit is set to one (1) when the bit Rdy/-Bsy changes state. This bit can also be written by the host.

Rdy/-Bsy: This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit can be used to determine the state of the RDY/-BSY as this pin has been reallocated for use as -IREQ on the I/O interface.

MRdy/-Bsy: This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

7.2.4 Socket and Copy Register (Offset 06h)

This register contains additional configuration information. The host must always set this register before writing configuration index to the Configuration Option Register.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Device #	0	0	0	0
Write	0	0	0	Device #	X	X	X	X

Reserved: This bit is reserved for future standards. This bit must be set to zero (0) by the host whenever the register is written.

Device #: This is always read as zero (0) and must be set to zero (0) as the IBM microdrive does not support twin card configuration.

X: the socket number field is ignored by the IBM microdrive.

7.3 ATA Register Set Definition

The IBM microdrive can be configured as an I/O device through

- Primary I/O mapped address spaces (1F0h - 1F7h, 3F6h - 3F7h) or secondary I/O mapped address spaces (170h - 177h, 376h - 377h)
- Contiguous I/O mapped address spaces; any system decoded 16-byte I/O block
- Memory mapped space
- True IDE mode; only I/O operations to the Task File and Data registers allowed, no PCMCIA functionality.

The communication to or from the card is done using the Task File registers which provide all the necessary registers for control and status information.

7.4 ATA Command Set

This section defines the format of the commands the host sends to the IBM microdrive. Commands are issued to the card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table below) of command acceptance, all dependent on the host not issuing commands unless the card is not busy (BSY=0).

- Upon receipt of a Class 1 command, the card sets BSY within 400 nsec.
- Upon receipt of a Class 2 command, the card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 usec, and clears BSY within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no re-assignments), and clears BSY within 400 nsec of setting DRQ.

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Device Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Device Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Standby	E2h or 96h	-	-	-	-	D	-

Figure 32. CF-ATA Command Set (1/2)

1	Standby Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Figure 33. CF-ATA Command Set (2/2)

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Device/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y - The register contains a valid parameter for this command. For the Device/Head Register Y means both the Card and head parameters are used; D - only the Card parameter is valid and not the head parameter.

7.4.1 Check Power Mode - 98h or E5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Device			X	
Cyl High (5)				X				
Cyl Low (4)				X				
Sec Num (3)				X				
Sec Cnt (2)				X				
Feature (1)				X				

This command checks the power mode.

If the card is in, going to, or recovering from the standby or sleep mode, the card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the card is in Idle mode, the card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

7.4.2 Execute Device Diagnostic - 90h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)		X		Device			X	
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command performs the internal diagnostic tests implemented by the card.

If in PCMCIA configuration this command runs only on the card which is addressed by the Device/Head register when the diagnostic command is issued. This is because PCMCIA card interface does not allow for direct inter-device communication (such as the ATA PDIAG and DASP signals). If in True IDE Mode the Device bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown below are returned in the Error Register at the end of the command.

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

Figure 34. Diagnostic Codes

7.4.3 Erase Sector(s) - C0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is implemented as a no-op command with access range validation as the IBM microdrive does not need pre-erase in advance of a write operation.

7.4.4 Format Track - 50h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

This command writes the desired head and cylinder of the selected drive with a data pattern (00h). To remain host backward compatible, the card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the card. If LBA=1 then the number of sectors to format is taken from the Sector Count register (0=256). The use of this command is not recommended.

7.4.5 Flush Cache - E7h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7h							
C/D/H (6)	X		Device		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command causes the card to complete writing data from its cache. The card returns status with RDY=1 and DSC=1 after data in the write cache buffer is written to the media.

7.4.6 Identify Device - ECh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Device		X		
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

The Identify Device command enables the host to receive parameter information from the card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in the following table. All reserved bits or words are zero.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash Storage Card
1	02B7h (0158h)	2	Default number of cylinders
2	0000h	2	Reserved
3	0010h	2	Default number of heads
4	7E00h	2	Number of unformatted bytes per track
5	0200h	2	Number of unformatted bytes per sector
6	003Fh	2	Default number of sectors per track
7-8	AB090h (54A80h)	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Vendor Unique
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0003h	2	Buffer type
21	00C0h	2	Buffer size in 512 byte increments
22	0004h	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8010h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double Word not supported
49	0E00h	2	Capabilities
50	0000h	2	Reserved
51	0100h	2	PIO data transfer cycle timing mode
52	0000h	2	DMA data transfer cycle timing mode
53	0001h	2	Translation parameters are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	AB090h (54A80h)	4	Total number of sectors addressable in LBA Mode
62-127	0000h	138	Reserved
128-159	0000h	64	Vendor unique bytes
160	8100h	2	Power requirement description
162-255	0000h	188	Reserved

Figure 35. Table 5-8 Identify Device Information

General Configuration

This field informs the device is a CompactFlash Storage Card.

Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Number of Unformatted Bytes per Track

This field contains the number of unformatted bytes per translated track in the default translation mode.

Number of Unformatted Bytes per Sector

This field contains the number of unformatted bytes per sector in the default translation mode.

Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Number of Sectors per Card

This field contains the number of sectors per card. This double word value is also the first invalid address in LBA translation mode.

Memory Card Serial Number

The contents of this field are right justified and padded with spaces (20h).

Buffer Type

This field defines the buffer capability:

0003h: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the Card with a read caching capability.

Buffer Size

This field defines the buffer capacity in 512 byte increments.

ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

Firmware Revision

This field contains the revision of the firmware for the IBM microdrive.

Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

Read/Write Multiple Sector Count

The even byte value of this field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

Double Word Support

This field indicates the IBM microdrive does not support double word transfers.

Capabilities

Bit 13 = 0 : Standby timer operation is IBM specific

Bit 11 = 1 : IORDY supported

Bit 10 = 1 : IORDY can be disabled

Bit 9 = 1 : LBA mode supported

Bit 8 = 0: DMA transfer not supported

PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer.

DMA Data Transfer Cycle Timing Mode

This field defines the mode for DMA data transfer.

Translation Parameters Valid

This field contains the value 0001h indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors.

Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Multiple Sector Setting

This field contains a validity flag in the odd byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the even byte. The odd byte is always 01h, which indicates that the even byte is always valid.

The even byte value depends on the value set by the Set Multiple command. The even byte of this word by default contains a 00h, which indicates that R/W Multiple commands are not valid.

Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the card in LBA mode only.

Power Requirement Description

Bit 15: VLD

if set to 1, indicates that this word contains valid power requirement description.

if set to 0, indicates that this word does not contain power requirement description.

Bit 14: RSV

This bit is reserved and must be 0.

Bit 13: -XP

if set to 1, indicates that the Card does not have Power Level 1 commands.

if set to 0, indicates that the Card has Power Level 1 commands

Bit 12: -XE

if set to 1, indicates that Power Level 1 commands are disabled..

if set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

This field contains the Card's maximum current in mA.

7.4.7 Idle - 97h or E3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X		Device		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Timer Count (5 sec increments)							
Feature (1)					X			

This command causes the card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 seconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

7.4.8 Idle Immediate - 95h or E1h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X		Device		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command causes the card to set BSY, enter the Idle mode, clear BSY and raise an interrupt.

7.4.9 Initialize Device Parameters - 91h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Device	Max Head (no. of heads-1)			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Number of Sectors							
Feature (1)					X			

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Device/Head registers are used by this command.

7.4.10 Read Buffer - E4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X		Device		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

The Read Buffer command enables the host to read the current contents of the card's sector buffer. This command has the same protocol as the Read Sector(s) command.

7.4.11 Read Multiple - C4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

$$n = (\text{sector count}) - \text{modulo}(\text{block count}).$$

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

7.4.12 Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

7.4.13 Read Sector(s) - 20h or 21h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

7.4.14 Read Verify Sector(s) - 40h or 41h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the card sets BSY.

When the requested sectors have been verified, the card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

7.4.15 Recalibrate - 1Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Device	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command moves the read/write heads from anywhere on the disk to cylinder 0. This is provided for compatibility purpose.

7.4.16 Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Device	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command requests extended error information for the previous command. Following table defines the valid extended error codes for the IBM microdrive. The extended error code is returned to the host in the Error Register.

Extended Error Code	Description
00h	No Error Detected
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
11h	Uncorrectable ECC Error
05h	Self Test or Diagnostic Failed
10h	ID Not Found
3Ah	Spare Sectors Exhausted
0Ch	Corrupted Media Format
03h	Write / Erase Failed
22h	Extended power operations disabled

Figure 36. Table 5-9 Extended Error Codes

7.4.17 Seek - 7Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command initiates a seek to the designated track and head. The card performs a range check of cylinder and head or LBA and returns an error if the address is out of range.

7.4.18 Set Features - EFh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X		Device		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Config			
Feature (1)					Feature			

This command is used by the host to establish or select certain features. Following table defines all features that are supported.

Feature	Operation
01h	Enable 8-bit data transfer.
02h	Enable Write Cache.
03h	Used for Set Transfer Mode command.
05h	Set Advanced Power Management mode.
09h	Enable Extended Power operations.
44h	Product specific ECC bytes (34 bytes) apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP ñ Accepted for backward compatibility.
81h	Disable 8-bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations
96h	NOP ñ Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	NOP ñ Accepted for backward compatibility.
AAh	Enable Read Look Ahead
BBh	4 bytes of ECC apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Figure 37. Features Supported

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers will occur on the low order D7-D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 82h, AAh and BBh are the default features for the IBM microdrive, thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults

will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

Features 09h and 89h are used to enable and disable Extended Power operations. Feature 09h is the default features for the card with extended power requirement.

Features 05h is used for advanced power management. The Sector Count Register specifies the advanced power management level as below. The advanced power management level at power on reset is 60h.

- 80h - FEhUp to Low Power Idle mode
- 01h - 7FhUp to Standby mode
- 00h, FFhReserved

Features 85h is used to disable advanced power management. This results in the same effect as the host uses features 05h with the Sector Count Register FEh.

7.4.19 Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)		X		Device			X	
Cyl High (5)					X			
Cyl Low (4)				X				
Sec Num (3)				X				
Sec Cnt (2)				Sector Count				
Feature (1)					X			

This command enables the card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the card sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

7.4.20 Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0	
Command (7)	99h or E6h								
C/D/H (6)	X		Device		X				
Cyl High (5)					X				
Cyl Low (4)					X				
Sec Num (3)					X				
Sec Cnt (2)					X				
Feature (1)					X				

Bit -> 7 6 5 4 3 2 1 0

This command causes the card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). The IBM microdrive treats Sleep mode as Standby mode.

7.4.21 Standby - 96h or E2h

Bit ->	7	6	5	4	3	2	1	0	
Command (7)	96h or E2h								
C/D/H (6)	X		Device		X				
Cyl High (5)					X				
Cyl Low (4)					X				
Sec Num (3)					X				
Sec Cnt (2)					X				
Feature (1)					X				

This command causes the card to enter the Standby mode immediately, and set Standby Timer. When this command is issued, the card confirms the completion of the cached write commands before it raises an interrupt. Then the card is spun down, but the interface remains active. If the card is already spun down, the spin down sequence is not executed. During the Standby mode the card will respond to commands, but there is a delay while waiting for the spindle motor to reach operating speed. The timer starts counting down when the card returns to Idle mode.

7.4.22 Standby Immediate - 94h or E0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)	X		Device		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command causes the card to enter Standby mode immediately. When this command is issued, the card confirms the completion of the cached write commands before raising an interrupt. Then the card is spun down, but the interface remains active. If the card is already spun down, the spin down sequence is not executed. During the Standby mode, the card will respond to commands, but there is a delay while waiting for the spindle motor to reach operating speed. This command does not affect the Standby Timer.

7.4.23 Translate Sector - 87h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)					X			
Feature (1)					X			

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that

sector. The following table represents the information in the buffer. Please note that this command is unique to the card.

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h - 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) ¹
1Bh-1FFh	Reserved

Figure 38. Translate Sector Information

Note 1: A value of 0 indicates Hot Count is not supported.

7.4.24 Wear Level - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Device	Flag			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Completion Status							
Feature (1)					X			

This command is implemented as a no-op command. However, the Sector Count Register is returned with 00h for backward compatibility.

7.4.25 Write Buffer - E8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X		Device		X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write Buffer command enables the host to overwrite contents of the card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

7.4.26 Write Long Sector - 32h or 33h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state Card, the four bytes of ECC transferred by the host may be used by the card. The card may discard these four bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

7.4.27 Write Multiple Command - C5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	X	LBA	X	Device	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write Sectors command. The card sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$n = \text{sector count (modulo sector/block)}.$$

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be trans-

ferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

7.4.28 Write Multiple without Erase - CDh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X	LBA	X	Device	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Write Multiple command as the IBM microdrive does not need pre-erase before a write operation.

7.4.29 Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

7.4.30 Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Write Sector(s) command as the IBM microdrive does not need pre-erase before a write operation.

7.4.31 Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Device	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The IBM microdrive handles Write Verify as the Write Sector(s) command. There is no implied verify operation.

7.4.32 Error Posting

The following table summarizes the valid status and error value for all the CF-ATA Command set.

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V		V	V	V		V
Execute						V		V		V
Device Diagnostic ¹										
Erase Sector(s)	V		V	V	V	V	V	V		V
Flush Cache			V	V	V	V		V		V
Format Track			V	V	V	V	V	V		V
Identify Device				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Device Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

Figure 39. Error and Status Register

Note: V = valid on this command

8.0 Appendix

8.1 Power mode definition

Active mode

The card is in execution of a command or accessing medium.

Performance Idle mode

The card usually enters this mode immediately after completing a command process in Active mode. In Performance Idle mode, all electronic components remain powered and full frequency servo remains operational. This provides instantaneous response to the next command.

Low Power Idle mode

Power consumption is 55%-65% less than that of Performance Idle mode. The heads are unloaded on the ramp, however the spindle is still rotating at the full speed.

Standby mode

The card interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle motor to reach operating speed.

Each power mode affects the physical interface as defined in the following table:

Power Mode	Read/Write	Servo	Head	Spindle Motor	Host Interface
Active	On	On	Loaded	On	On
Performance Idle	Off	On	Loaded	On	On
Low Power Idle	Off	Off	Unloaded	On	On
Standby	Off	Off	Unloaded	Off	On

8.2 Power management commands

Check Power Mode

The Check Power Mode command allows a host to determine if a card is currently in, going to or leaving standby mode. Upon completion of the Check Power Mode command the card sets 00h to the Sector Count Register if the device is in standby mode, otherwise the card sets FFh to the Sector Count Register.

Idle and Idle Immediate

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

Sleep

The Sleep command moves a card to standby mode.

Standby and Standby Immediate

The Standby and Standby Immediate commands move a card to standby mode immediately from the

active or idle modes. The standby command also sets the standby timer count.

Standby/Sleep command completion timing

The card enters Standby or Sleep mode in response to Standby Immediate or Sleep command as following sequence:

- Confirm the completion of writing cached data in the buffer to media

- Unload heads on the ramp

- Set DRDY bit and DSC bit in Status Register

- Assert INTRQ (command completion)

- Activate the spindle break to stop the spindle motor

- Wait until spindle motor is stopped

Standby Timer

The standby timer provides a method for the card to automatically enter standby mode from either active or idle mode following a host's programmed period of inactivity. If the card is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode. If the value of Sector Count Register on Idle or Standby command is set to 00h, the card will automatically set the standby timer to 109 minutes.

8.3 Card Information Structure

Addr	Value	Description
00	01	; CI STPL_DEVICE (5V Device Information Tuple)
02	03	; Tuple length = 4 bytes
		; Device Info fields
04	D9	; Device ID
		; Device Type (bit4..7) = D (DTYPE_FUNCSPEC)
		; WPS(write protect switch) (bit3) = 1 (non WP)
		; Device Speed (bit0..2) = 1 (DSPEED_250NS)
06	01	; Device Size = 1 (2K bytes)
08	FF	; End Mark

0A	1C	; CI STPL_DEVICE_OC (Additional Device Information Tuple)
0C	04	; Tuple length = 4 bytes
0E	03	; Other Condition Info
		; Ext (bit7) = 0
		; Reserved (bit3..6) = 0
		; Vcc Used (bit1,2) = 1 (3.3V)
		; MWAIT (bit0) = 1
		; Device Info fields
10	D9	; Device Information
		; Device Type (bit4..7) = D (DTYPE_FUNCSPEC)
		; WPS(write protect switch) (bit3) = 1 (non WP)
		; Device Speed (bit0..2) = 1 (DSPEED_250NS)
12	01	; Device Size Code = 1 (2K bytes)
14	FF	; End Mark

16	18	; CI STPL_JEDEC_C (JEDEC ID Tuple)
18	02	; Tuple length = 2 bytes
1A	DF	; PC Card ATA with no Vpp required for any operation
1C	01	;

1E	20	; CI STPL_MANFID (Manufacture ID Tuple)
20	04	; Tuple length = 4 bytes
22	A4	; TPLMID_MANF (Manufacture Code) = 00A4h for IBM
24	00	; v
26	00	; TPLMID_CARD (Manufacture Info)
28	00	; v

2A	15	; CI STPL_VERS_1 (Level 1 Version Tuple)
2C	12	; Tuple length = 17h bytes
2E	04	; Major Version = 4 (JEIDA 4.2/PCMCIA 2.1)
30	01	; Minor Version = 1 v
32	"IBM"	;
38	00	;
3A	"microdrive"	;
4E	00	;
50	FF	; End mark

```

-----
52    21 ; CISTPL_FUNCID (Function ID Tuple)
54    02 ; Tuple length = 2 bytes
56    04 ; TPLFID_FUNCTION (IC Card function code) = 04 (Fixed Disk)
58    01 ; TPLFID_SYSINIT (System Initialization bit mask)
      ;     POST(bit0) = 1
      ;     ROM (bit1) = 0
-----

5A    22 ; CISTPL_FUNCNCE (Function Extension Tuple)
5C    02 ; Tuple length = 2 bytes
5E    01 ; TPLFCE_TYPE (Extension Type) = 01 (Disk Device Interface)
60    01 ; TPLFCE_DATA (Interface Type) = 01 (PC Card ATA Interface)
-----

62    22 ; CISTPL_FUNCNCE (Function Extension tuple)
64    03 ; Tuple length = 3 bytes
66    02 ; TPLFCE_TYPE (Extension Type) = 02 (Basic PC Card ATA Interface)
68    08 ; TPLFCE_DATA
      ;     V : Vpp[2:1] (bit0,1) = 00 (Vpp not required)
      ;     S : Silicon (bit2) = 0 (Rotating device)
      ;     U : Unique (bit3) = 1 (Model/Serial is unique)
      ;     D : Dual drive (bit4) = 0 (single drive)
6A    2F ; TPLFCE_DATA
      ;     P0 : Sleep (bit0) = 1 (support sleep mode)
      ;     P1 : Standby (bit1) = 1 (support standby mode)
      ;     P2 : Idle (bit2) = 1 (support idle mode)
      ;     P3 : Auto (bit3) = 1 (support automatic power control)
      ;     N : 3F7/377 (bit4) = 0 (include 3F7h 377h for I/O address)
      ;     E : Index Emulate (bit5) = 1 (index emulation is supported)
      ;     I : IOIS16 (bit6) = 0
-----

6C    1A ; CISTPL_CONFIG (Configuration Tuple)
6E    05 ; Tuple length = 5 bytes
70    01 ; TPCC_SZ (Size of Fields Byte)
      ;     TPCC_RASZ (Size of TPCC_RADR) (bit0,1) = 1 (2bytes)
      ;     TPCC_RMSZ (Size of TPCC_RMSK) (bit2..5) = 0 (1byte)
72    07 ; TPCC_LAST (Last Entry Index) = 07
74    00 ; TPCC_RADR (Base address of Configuration Register) = 0200h
76    02 ; v
78    0F ; TPCC_RMSK (Register Presence Mask) = 00001111b (200, 202, 204, 206)
-----

7A    1B ; CISTPL_CFTABLE_ENTRY (16bit PCCard Configuration Table Entry Tuple)
7C    0B ; Tuple length = 0Bh bytes
7E    C0 ; TPCE_INDX (Configuration Table Index Byte)
      ;     Config Entry Number (bit0..5) = 00 (Memory Mode)
      ;     Default (bit6) = 1
      ;     Interface (bit7) = 1 (interface field exist)
80    C0 ; TPCE_IF (Interface Description Field)
      ;     Interface Type (bit0..3) = 00 (Memory)
      ;     BVDs active (bit4) = 0
      ;     WP active (bit5) = 0
      ;     READY active (bit6) = 1

```

```

;      M Wait required (bi t7) = 1
82  A1 ; TPCE_FS (Feature Selecti on byte)
;      Power      (bi t0,1) = 01 (Vcc onl y)
;      Timing    (bi t2) = 0
;      I/O       (bi t3) = 0
;      Interrupt  (bi t4) = 0
;      Memory    (bi t5,6) = 01
;      Misc      (bi t7) = 1
;      TPCE_PD (Power Descripti on Structure)
84  27 ; Parameter Selecti on Byte
;      NomV      (bi t0) = 1
;      MinV      (bi t1) = 1
;      MaxV      (bi t2) = 1
;      PeakI     (bi t5) = 1
86  55 ; Power Parameter Defini ti on (NomV)
;      Exponent  (bi t0..2) = 5 (1V)      --> 5.0 V
;      Mantissa  (bi t3..6) = A (5.0)
88  4D ; Power Parameter Defini ti on (Mi nV)
;      Exponent  (bi t0..2) = 5 (1V)      --> 4.5 V
;      Mantissa  (bi t3..6) = 9 (4.5)
8A  5D ; Power Parameter Defini ti on (MaxV)
;      Exponent  (bi t0..2) = 5 (1V)      --> 5.5 V
;      Mantissa  (bi t3..6) = C (5.5)
8B  4E ; Power Parameter Defini ti on (PeakI)
;      Exponent  (bi t0..2) = 6 (100mA)  --> 450 mA
;      Mantissa  (bi t3..6) = 9 (4.5)
;      TPCE_MS (Memory Space Descripti on Structure)
8C  08 ; Memory Space Descrip tor Byte
;      # of Windo ws (-1) (bi t0..2) = 0 (# of windo w = 1)
;      Length Si ze (bi t3..4) = 1 (length fi eld si ze = 1 byte)
;      Card Addr Si ze (bi t5..6) = 0 (no card addr fi eld)
;      Host Addr    (bi t7) = 0 (arbi trary host addr)
8E  00 ; Window Descrip tor
;      Length of the windo w = 0
90  20 ; TPCE_MI (Mi scel laneous Features Fi eld)
;      Max Twin Card (bi t0..2) = 0
;      Audi o (bi t3) = 0
;      Read Onl y (bi t4) = 0
;      Power Down (bi t5) = 1 (support power down mode)

-----
92  1B ; CI STPL_CFTABLE_ENTRY (16bi t PCCard Configurati on Table Entry Tupl e)
94  06 ; Tupl e length = 06h bytes
96  00 ; TPCE_I_NDX (Configurati on Table Index Byte)
;      Config Entry Number (bi t0..5) = 00 (Memory Mode)
;      Defaul t (bi t6) = 0
;      Interface (bi t7) = 0 (i nterface fi eld existi)
98  01 ; TPCE_FS (Feature Selecti on byte)
;      Power      (bi t0,1) = 01 (Vcc onl y)
;      Timing    (bi t2) = 0
;      I/O       (bi t3) = 0
;      Interrupt  (bi t4) = 0
;      Memory    (bi t5,6) = 00
;      Misc      (bi t7) = 0
9A  21 ; Parameter Selecti on Byte
;      NomV      (bi t0) = 1
;      MinV      (bi t1) = 0
;      MaxV      (bi t2) = 0

```

```

;          PeakI (bi t5) = 1
9C   B5 ;          Power Parameter Defini ti on (NomV)
;          Exponent   (bi t0..2) = 5 (1V)          ---> 3.3 V
;          Manti ssa   (bi t3..6) = 6 (3.0)        +
;          Extensi on   (bi t7) = 1 (extensi on exists) +
9E   1E ;          Extensi on           = 1Eh = +0.30  ---+
A0   3E ;          Power Parameter Defini ti on (PeakI)
;          Exponent   (bi t0..2) = 6 (100mA)      --> 350 mA
;          Manti ssa   (bi t3..6) = 7 (3.5)

```

```

-----
A2   1B ; CI STPL_CFTABLE_ENTRY (16bi t PCCard Configurati on Table Entry Tupl e)
A4   0D ; Tupl e length = 0Dh bytes
A6   C1 ; TPCE_INDX (Configurati on Table Index Byte)
;          Config Entry Number (bi t0..5)= 01 (I/O and Memory Mode)
;          Default           (bi t6) = 1
;          Interface         (bi t7) = 1 (i nterface fi eld exist)
A8   41 ; TPCE_IF (Interface Descripti on Fi eld)
;          Interfece Type (bi t0..3) = 01 (I/O and Memory)
;          BVDs active (bi t4) = 0
;          WP active (bi t5) = 0
;          READY active (bi t6) = 1
;          M Wait required (bi t7) = 0
AA   99 ; TPCE_FS (Feature Selecti on byte)
;          Power (bi t0,1) = 01 (Vcc onl y)
;          Timi ng (bi t2) = 0
;          I/O (bi t3) = 1
;          Interrupt (bi t4) = 1
;          Memory (bi t5,6) = 00
;          Misc (bi t7) = 1
;          TPCE_PD (Power Descripti on Structure)
AC   27 ;          Parameter Selecti on Byte
;          NomV (bi t0) = 1
;          Mi nV (bi t1) = 1
;          MaxV (bi t2) = 1
;          PeakI (bi t5) = 1
AE   55 ;          Power Parameter Defini ti on (NomV)
;          Exponent (bi t0..2) = 5 (1V)          --> 5.0 V
;          Manti ssa (bi t3..6) = A (5.0)
B0   4D ;          Power Parameter Defini ti on (Mi nV)
;          Manti sa (bi t0..2) = 5 (1V)          --> 4.5 V
;          Exponent (bi t3..6) = 9 (4.5)
B2   5D ;          Power Parameter Defini ti on (MaxV)
;          Exponent (bi t0..2) = 5 (1V)          --> 5.5 V
;          Manti ssa (bi t3..6) = C (5.5)
B4   4E ;          Power Parameter Defini ti on (PeakI)
;          Exponent (bi t0..2) = 6 (100mA)      --> 450 mA
;          Manti ssa (bi t3..6) = 9 (4.5)
B6   64 ; TPCE_I0 (I/O space address required for thi s configurati on)
;          IO Address Lines (bi t0..4) = 4 (16byte boundary)
;          Bus 16/8 (bi t 5,6) = 3 (support 16/8 bi t access)
;          Range (bi t 7) = 0
;          TPCE_IR (Interrupt Request Descripti on structure)
B8   F0 ;          IRQ line 0..15 (bi t0..3) = 0
;          MASK (bi t4) = 1
;          Level (bi t5) = 1
;          Pul se (bi t6) = 1
;          Share (bi t7) = 1

```

```

BA    FF ; IRQ0..IRQ7 = all supported
BC    FF ; IRQ8..IRQ15 = all supported
BE    20 ; TPCE_MI (Miscellaneous Features Field)
        ; Max Twin Card (bit0..2) = 0
        ; Audio (bit3) = 0
        ; Read Only (bit4) = 0
        ; Power Down (bit5) = 1 (support power down mode)
-----
C0    1B ; CISTPL_CFTABLE_ENTRY (16bit PCCard Configuration Table Entry Tuple)
C2    06 ; Tuple Length = 06h bytes
C4    01 ; TPCE_INDX (Configuration Table Index Byte)
        ; Config Entry Number (bit0..5) = 01 (I/O and Memory Mode)
        ; Default (bit6) = 0
        ; Interface (bit7) = 0 (interface field exist)
C6    01 ; TPCE_FS (Feature Selection byte)
        ; Power (bit0,1) = 01 (Vcc only)
        ; Timing (bit2) = 0
        ; I/O (bit3) = 0
        ; Interrupt (bit4) = 0
        ; Memory (bit5,6) = 00
        ; Misc (bit7) = 0
        ; TPCE_PD (Power Description Structure)
C8    21 ; Parameter Selection Byte
        ; NomV (bit0) = 1
        ; MinV (bit1) = 0
        ; MaxV (bit2) = 0
        ; PeakI (bit5) = 1
CA    B5 ; Power Parameter Definition (NomV)
        ; Exponent (bit0..2) = 5 (1V) ---+> 3.3 V
        ; Mantissa (bit3..6) = 6 (3.0) +
        ; Extension (bit7) = 1 (extension exists) +
CC    1E ; Extension = 1Eh = +0.30 ---
CE    3E ; Power Parameter Definition (PeakI)
        ; Exponent (bit0..2) = 6 (100mA) --> 350 mA
        ; Mantissa (bit3..6) = 7 (3.5)
-----
D0    1B ; CISTPL_CFTABLE_ENTRY (16bit PCCard Configuration Table Entry Tuple)
D2    12 ; Tuple Length = 12h bytes
D4    C2 ; TPCE_INDX (Configuration Table Index Byte)
        ; Config Entry Number (bit0..5) = 02 (I/O Primary Mode)
        ; Default (bit6) = 1
        ; Interface (bit7) = 1 (interface field exist)
D6    41 ; TPCE_IF (Interface Description Field)
        ; Interface Type (bit0..3) = 01 (I/O and Memory)
        ; BVDs active (bit4) = 0
        ; WP active (bit5) = 0
        ; READY active (bit6) = 1
        ; M Wait required (bit7) = 0
D8    99 ; TPCE_FS (Feature Selection byte)
        ; Power (bit0,1) = 01 (Vcc only)
        ; Timing (bit2) = 0
        ; I/O (bit3) = 1
        ; Interrupt (bit4) = 1
        ; Memory (bit5,6) = 00
        ; Misc (bit7) = 1
        ; TPCE_PD (Power Description Structure)
DA    27 ; Parameter Selection Byte

```

```

;      NomV (bi t0) = 1
;      Mi nV (bi t1) = 1
;      MaxV (bi t2) = 1
;      PeakI (bi t5) = 1
DC    55 ;      Power Parameter Defini ti on (NomV)
;      Exponent (bi t0..2) = 5 (1V)          --> 5.0 V
;      Manti ssa (bi t3..6) = A (5.0)
DE    4D ;      Power Parameter Defini ti on (Mi nV)
;      Exponent (bi t0..2) = 5 (1V)          --> 4.5 V
;      Manti ssa (bi t3..6) = 9 (4.5)
EO    5D ;      Power Parameter Defini ti on (MaxV)
;      Exponent (bi t0..2) = 5 (1V)          --> 5.5 V
;      Manti ssa (bi t3..6) = C (5.5)
E2    4E ;      Power Parameter Defini ti on (PeakI)
;      Exponent (bi t0..2) = 6 (100mA)       --> 450 mA
;      Manti ssa (bi t3..6) = 9 (4.5)
E4    EA ;      TPCE_I0 (I/O space address required for this configuration)
;      IO Address Lines (bi t0..4) = A (1Kbyte boundary)
;      Bus 16/8 (bi t 5,6) = 3 (support 16/8 bit access)
;      Range (bi t 7) = 1 (see range rescripti on)
E6    61 ;      I/O range descri pti on byte
;      # of address range -1 (bi t0..3) = 1 (# of fi eld = 2)
;      size of address (bi t 4,5) = 2 (2byte address)
;      size of length (bi t 6,7) = 1 (1byte length)
E8    F0 ;      I/O address range descri pti on fi eld #1 address = 1F0
EA    01 ;      |
EC    07 ;      V address block length = 8
EE    F6 ;      I/O address range descri pti on fi eld #2 address = 3F6
FO    03 ;      |
F2    01 ;      V address block length = 2
F4    EE ;      TPCE_IR (Interrupt Request Descri pti on structure)
;      IRQ line 0..15 (bi t0..3) = E ??
;      MASK (bi t4) = 0
;      Level (bi t5) = 1
;      Pulse (bi t6) = 1
;      Share (bi t7) = 1
F6    20 ;      TPCE_MI (Mi scel laneous Features Fi eld)
;      Max Twin Card (bi t0..2) = 0
;      Audi o (bi t3) = 0
;      Read Only (bi t4) = 0
;      Power Down (bi t5) = 1 (support power down mode)

-----
F8    1B ;      CI STPL_CFTABLE_ENTRY (16bi t PCCard Configurati on Table Entry Tupl e)
FA    06 ;      Tupl e length = 06h bytes
FC    02 ;      TPCE_I_NDX (Configurati on Table Index Byte)
;      Config Entry Number (bi t0..5)= 02 (I/O Pri mary Mode)
;      Defaul t (bi t6) = 0
;      Interface (bi t7) = 0 (i nterface fi eld exist)
FE    01 ;      TPCE_FS (Feature Selecti on byte)
;      Power (bi t0,1) = 01 (Vcc onl y)
;      Timi ng (bi t2) = 0
;      I/O (bi t3) = 0
;      Interrupt (bi t4) = 0
;      Memory (bi t5,6) = 00
;      Mi sc (bi t7) = 0
;      TPCE_PD (Power Descri pti on Structure)
100   21 ;      Parameter Selecti on Byte

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```

;      NomV (bi t0) = 1
;      Mi nV (bi t1) = 0
;      MaxV (bi t2) = 0
;      PeakI (bi t5) = 1
102   B5 ;      Power Parameter Defini ti on (NomV)
;      Exponent (bi t0..2) = 5 (1V)          ---> 3.3 V
;      Manti ssa (bi t3..6) = 6 (3.0)        +
;      Extensi on (bi t7) = 1 (extensi on exists) +
104   1E ;      Extensi on = 1Eh = +0.30      ---
108   3E ;      Power Parameter Defini ti on (PeakI)
;      Exponent (bi t0..2) = 6 (100mA)      --> 350 mA
;      Manti ssa (bi t3..6) = 7 (3.5)
-----
10A   1B ;      CI STPL_CFTABLE_ENTRY (16bi t PCCard Configurati on Table Entry Tupl e)
10C   12 ;      Tupl e length = 12h bytes
10E   C3 ;      TPCE_I_NDX (Configurati on Table Index Byte)
;      Config Entry Number (bi t0..5)= 03 (I/O Secondary Mode)
;      Default (bi t6) = 1
;      Interface (bi t7) = 1 (interf ace fi eld exists)
110   41 ;      TPCE_I_F (Interf ace Descri pti on Fi eld)
;      Interf ace Type (bi t0..3) = 01 (I/O and Memory)
;      BVDS active (bi t4) = 0
;      WP active (bi t5) = 0
;      READY active (bi t6) = 1
;      M Wait required (bi t7) = 0
112   99 ;      TPCE_FS (Feature Selecti on byte)
;      Power (bi t0,1) = 01 (Vcc only)
;      Timi ng (bi t2) = 0
;      I/O (bi t3) = 1
;      Interrupt (bi t4) = 1
;      Memory (bi t5,6) = 00
;      Mi sc (bi t7) = 1
;      TPCE_PD (Power Descri pti on Structure)
114   27 ;      Parameter Selecti on Byte
;      NomV (bi t0) = 1
;      Mi nV (bi t1) = 1
;      MaxV (bi t2) = 1
;      PeakI (bi t5) = 1
116   55 ;      Power Parameter Defini ti on (NomV)
;      Exponent (bi t0..2) = 5 (1V)          --> 5.0 V
;      Manti ssa (bi t3..6) = A (5.0)
118   4D ;      Power Parameter Defini ti on (Mi nV)
;      Exponent (bi t0..2) = 5 (1V)          --> 4.5 V
;      Manti ssa (bi t3..6) = 9 (4.5)
11A   5D ;      Power Parameter Defini ti on (MaxV)
;      Exponent (bi t0..2) = 5 (1V)          --> 5.5 V
;      Manti ssa (bi t3..6) = C (5.5)
11C   4E ;      Power Parameter Defini ti on (PeakI)
;      Exponent (bi t0..2) = 6 (100mA)      --> 450 mA
;      Manti ssa (bi t3..6) = 9 (4.5)
11E   EA ;      TPCE_I_O (I/O space address required for thi s configurati on)
;      I/O Address Lines (bi t0..4) = A (1Kbyte boundary)
;      Bus 16/8 (bi t 5,6) = 3 (support 16/8 bi t access)
;      Range (bi t 7) = 1 (see range rescri pti on)
120   61 ;      I/O range descri pti on byte
;      # of address range -1 (bi t0..3) = 1 (# of fi eld = 2)
;      size of address (bi t 4,5) = 2 (2byte address)
;      size of length (bi t 6,7) = 1 (1byte length)
122   70 ;      I/O address range descri pti on fi eld #1 address = 170

```

```

124 01 ; |
126 07 ; V address block length = 8
128 76 ; I/O address range description field #2 address = 376
12A 03 ; |
12C 01 ; V address block length = 2
12E EE ; TPCE_IR (Interrupt Request Description structure)
; IRQ line 0..15 (bit0..3) = E
; MASK (bit4) = 0
; Level (bit5) = 1
; Pulse (bit6) = 1
; Share (bit7) = 1
130 20 ; TPCE_MI (Miscellaneous Features Field)
; Max Twin Card (bit0..2) = 0
; Audio (bit3) = 0
; Read Only (bit4) = 0
; Power Down (bit5) = 1 (support power down mode)
-----
132 1B ; CISTPL_CFTABLE_ENTRY (16bit PCCard Configuration Table Entry Tuple)
134 06 ; Tuple length = 06h bytes
136 03 ; TPCE_INDX (Configuration Table Index Byte)
; Config Entry Number (bit0..5) = 03 (I/O Secondary Mode)
; Default (bit6) = 0
; Interface (bit7) = 0 (interface field exist)
138 01 ; TPCE_FS (Feature Selection byte)
; Power (bit0,1) = 01 (Vcc only)
; Timing (bit2) = 0
; I/O (bit3) = 0
; Interrupt (bit4) = 0
; Memory (bit5,6) = 00
; Misc (bit7) = 0
; TPCE_PD (Power Description Structure)
13A 21 ; Parameter Selection Byte
; NomV (bit0) = 1
; MinV (bit1) = 0
; MaxV (bit2) = 0
; PeakI (bit5) = 1
13C B5 ; Power Parameter Definition (NomV)
; Mantissa (bit0..2) = 5 (1V) ---+> 3.3 V
; Exponent (bit3..6) = 6 (3.0) +
; Extension (bit7) = 1 (extension exists) +
13E 1E ; Extension = 1Eh = +0.30 ---+
140 3E ; Power Parameter Definition (PeakI)
; Exponent (bit0..2) = 6 (100mA) --> 350 mA
; Mantissa (bit3..6) = 7 (3.5)
-----
142 14 ; CISTPL_NO_LINK (No Link Tuple)
144 00 ; Tuple length = 0 bytes
-----
146 FF ; CISTPL_END (Tuple End)

```

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